

SRI BHARATHI

ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai)

Kaikkurichi, Pudukkottai -622 303

www.sbec.edu.in

NAAC DOCUMENTS



Quality Indicator Frame Work

Criterion – 2

Teaching-Learning and Evaluation

Submitted by

IQAC
Internal Quality Assurance Cell

Sri Bharathi Engineering College for Women

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Criteria 2

Teaching-Learning and Evaluation

350

Key Indicator- 2.3. Teaching- Learning Process (40)

2018-2019

ELECTRONICS AND COMMUNICATION ENGINEERING

PARTICIPATIVE LEARNING

Activity	Number of Students Attended	Page No.
Value Added Course (VAC)	100	3
Workshop	19	53
TOTAL STUDENTS ATTENDED	119	-

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Criteria 2

Teaching-Learning and Evaluation

350

Key Indicator- 2.3. Teaching- Learning Process (40)

2018-2019

ELECTRONICS AND COMMUNICATION ENGINEERING PARTICIPATIVE LEARNING

VALUE ADDED COURSE



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu - 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

DEPARTMENT CIRCULAR

Date:08.06.2018

Value Added Course offered by the Department of ECE will be conducted for all Second, Third and Final year students on "Digital System Design with Xilinx" in association with Maria Academy from 18.06.2018 to 22.06.2018. Certificates will be issued to the eligible participants at the end of the course.

S.No	Name of the Course	Resource Person
1	Digital System Design with Xilinx	Er.A.GANESAN, Software Engineer, Maria Academy, No 58, 17, S Usman Road, Near Bus stand, Kannammapet, T. Nagar, Chennai 600059. Tamil Nadu . Mail.Id: mariatrainingacademy@gmail.com

Cc:

Principal's Office

IQAC Coordinator

II ,III & IV Year ECE Students

Notice Board

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI.

PUDUKKOTTAI - 622 303.

Class In charges- II ,III &IV Year Dr. S.THILAGAVATHIM.E. Ph.D., PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING <u>ACADEMIC YEAR 2018-2019/ODD SEMESTER</u>

Value Added Course on "Digital System Design With Xilinx"

SYLLABUS

S.NO	TOPIC COVERED	DURATION (in hours)	DATE
1	Evolution and Basics of ICs and Digital System Design, Evolution of Integrated Circuits ,Digital Logic Family	2	18.06.2018
2	Basics of Logic gates – Boolean Algebra – Digital circuit design using Boolean Algebra and K – Map.	1	18.06.2018
3	ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques.	3	18.06.2018
4	Architecture of ROM – ROM Programming – Architecture of SPLDs – SPLDs programming	3	19.06.2018
5	Architecture of CPLDs – Basics of FPGAs– Structure of FPGAs	3	19.06.2018
6	Verilog Coding and Simulation of Digital Systems using Xilinx	3	20.06.2018
7	Verilog HDL Basics- Gate level, Data flow and Behaviour Modelling – Simulation of simple digital circuits	3	20.06.2018
8	Implementation of Digital circuits in FPGA processor Spartan 6 FPGA features	3	21.06.2018
9	Education FPGA kit – FPGA pin assignment	3	21.06.2018
10	Implementation of simple digital circuits using FPGA hardware	3	22.06.2018
11	Interfacing Input /Output devices with FPGA	3	22.06.2018
	Total Hours	3	0

VACCoordinator

Dr. S.THILAGAVATHIME, Ph.D.

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 522 303, Pudukkottai Dt. HoD/ECE

HARATHI ENGINEER WALLEGE FOR WOMEN KAIKKURICHI



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DEPARTMENT OF ELECTRONICS AN COMMUNICATIONENGINEERING ACADEMIC YEAR ODD SEMESTER (2018-2019)

STUDENT PARTICIPATION LIST FOR VALUE ADDED PROGRAM

Digital System Design With Xilinx

S.NO	REG.NO	NAME	YEAR & BRANCH
11036	912617106001	ABIRAMI.S	II&ECE
2	912617106002	ABISHEKA.S	II&ECE
3	912617106003	ATSHAYA.R	II&ECE
4	912617106004	BAVADHARANI.A	II&ECE
5	912617106005	BHUVANESHWARI.B	II&ECE
6	912617106006	DHIVYA.L	II&ECE
7	912617106007	GOWSALYA.D	II&ECE
8	912617106009	INDHUMATHI.S	II&ECE
9	912617106010	KANIMOZHI.D	II&ECE
10	912617106011	KAVYA.C	II&ECE
11	912617106012	KEERTHANA.G	II&ECE
12	912617106013	MAHESHWARI.G	II&ECE
13	912617106014	MANOHARI.M	II&ECE
14	912617106015	MARAGATHALAKSHMI.S	II&ECE
15	912617106017	SAFRIN NISHA.S	II&ECE
16	912617106018	SUBASHINI.M	II&ECE
17	912617106019	SUBASHINI.T	II&ECE
18	912617106020	VINTHIYA.R	II&ECE
19	912616106001	ABINAYA.R	III&ECE
20	912616106002	AGALYA.A	III&ECE
21	912616106003	ATCHAYA.G	III&ECE
22	912616106004	DEEPA.N	III&ECE
23	912616106005	DHARANIYA.A	III&ECE
24	912616106006	JEEVITHA.U	III&ECE
25	912616106007	MAHESWARI . THILAGA	VATHI &HCE

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi- 622 303, Pudukkottai Dt.

S.NO	REG.NO	NAME	YEAR & BRANCH
26	912616106008	PAZHANIYAMMAL.R	III &ECE
27	912616106009	PRIYANKA.E	III &ECE
28	912616106010	ROJA.A	III &ECE
29	912616106011	SHANMUGAPRIYA.R	III &ECE
30	912616106012	SHIYAMALA.E	III&ECE
31	912616106013	SIVA BHARATHI.P	III&ECE
32	912616106014	SIVARUBINI.S	III&ECE
33	912616106015	THENMOZHI.A	III&ECE
34	912616106016	VINCY.A	III&ECE
35	912616106302	SANKAVI M	III&ECE
36	912615106001	AARTHI .M	IV&ECE
37	912615106002	ABIRAMI .C	IV&ECE
38	912615106004	AKILA .S	IV&ECE
39	912615106005	ARTHI .M	IV&ECE
40	912615106006	BAVADHARANI .M	IV&ECE
41	912615106007	DIVYABHARATHI .S	IV&ECE
42	912615106008	JAGADESWARI .K	IV&ECE
43	912615106009	MEENAKSHI .R	IV&ECE
44	912615106010	MEENAL.T	IV&ECE
45	912615106012	SARGUNAVALLI .C	IV&ECE
46	912615106013	THENMOZHI.K	IV&ECE
47	912615106014	VENNILA .K	IV&ECE
48	912615106301	MANIMEGALAI .S	IV&ECE
49	912615106701	SARADHA .S	IV&ECE
50	912615106702	KAVIYA. S	IV&ECE

VAC Coordinator

H₀D/ECE

HOD / ECE

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI, PUDUKKOTTAI - 622 303

Dr. S.THILAGAVATHI M.E., Ph.D.,

PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING ACADEMIC YEAR ODD SEMESTER (2018-2019)

ATTENDANCE SHEET FOR VALUE ADDED COURSE -DIGITAL SYSTEM DESIGN WITH XILINX

S.No	REG. NO	NAME	YEAR/	18.6.	.2018	19.6.	2018	20.6	2018	21.6.	2018	22.6	.2018	NO. OF	SIGN OF
-51		, mexitavn	BRANCH	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	SESSIONS ATTENDED	STUDENT
1	912617106001	ABIRAMI.S	II /ECE	1	1	1	,	1	1	1	1	,	1	10	S. Abiran
2	912617106002	ABISHEKA.S	II /ECE	1	1	1	1	1	1	1	,	,	,	10	s. De
3	912617106003	ATSHAYA.R	II /ECE	a	1	,	,	,	,	,	1	/	,	9	R. Atch
4	912617106004	BAVADHARANI.A	II /ECE	a	1	1	1	,	,	,	,	1	,	9	6. Baralle
5	912617106005	BHUVANESHWARI.B	II /ECE	1	1	,	,	1	/	,	,	1	,		B'Bhuvane
6	912617106006	DHIVYA.L	II /ECE	1	,	,	,	1	1	,	,	1	,	10	J Diver
7	912617106007	GOWSALYA.D	II /ECE	1	1	,	,	7	,	,	,	1	1	lp	D. Curred
8	912617106009	INDHUMATHI.S	II /ECE	,	/	1	,	a	,	,	,	,	1	9	S. Indlum
9	912617106010	KANIMOZHI.D	II /ECE	,	1	1	,	1	7	,	,	,	,	10	0
10	912617106011	KAVYA.C	II /ECE	/	,	,	1	1	,	,	,	1	,		D. Kanime
1.1	912617106012	KEERTHAN OGS. THIL	AGIA ECENI PRINCIPAL	M.E.,P	h.D.,	,	,	1	,	,	,	,	1	10	C. Kary
12	912617106013	MAHESHWARI. GRIBHA	RATH/BENEGIN EGE FOR WO	EERIN DMEN	G /	,	,	/	,	,	,	,	,		G. Koerthou G. Maliosco

13	912617106014	MANOHARI.M	II /ECE	1	1	,	1	1	1	1	1	1	1	10	M. Newing
14	912617106015	MARAGATHA LAKSHMI.S	II /ECE	a	a	1	1	1	1	,	1	,	1	8	S. Masageth
15	912617106017	SAFRIN NISHA.S	II /ECE	1	1	1	1	1	,	,	1	1	1	10	S. Safan Ri
16	912617106018	SUBASHINI.M	II /ECE	1	1	1	1	1	1	1	1	1	1	10	M. Subashi
17	912617106019	SUBASHINI.T	II /ECE	1	1	1	1	a	a	1	1	,	1	8	T. Subi
18	912617106020	VINTHIYA.R	II /ECE	1	,	,	,	1	,	1)	1	1	10	Rivinta
19	912616106001	ABINAYA.R	III/ECE	1	,	,	1	1	1	,)	1	1	10	R. Abiney
20	912616106002	AGALYA.A	III/ECE	a	a	,	1	1	1	1	1	,	1	8	A. Abgalya
21	912616106003	ATCHAYA.G	III/ECE	1	/	1	1	1	1	1	1	1	1	10	6. Atchas
22	912616106004	DEEPA.N	III/ECE	1	1	,	,	1	1	1	1	1	1	10	X. Doega
23	912616106005	DHARANIYA.A	III/ECE	1	1	1	1	a	,	1	1	1	1	9	A. Dharayo
24	912616106006	JEEVITHA.U	III/ECE	1	,	1	1	1	1	1	1	1	,	10	U. Feerith
25	912616106007	MAHESWARI.V	III/ECE	,	1	1	1	a	a	,	,	1	1	8	V. Maheur
26	912616106008	PAZHANIYAMMAL.R	III/ECE	,	,	,	1	1	1	1	,	,	/	10	Paghous
27	912616106009	PRIYANKA.E	III/ECE	1	,	1	,	1	,	1	1	1	1	10	Poryant
28	912616106010	ROJA.A	III/ECE	1	,	1	1	1	,	1	1	,	/	10	Rote
29	912616106011	SHANMUGAPRIYA.R	III/ECE	1	,	,	,	1	1.	1	1	1	1	10	Strawpaya
30	912616106012	SHIYAMALA.E	III/ECE	1	,	1	1	1	1	.,	1	1	1	10	E. Quet
31	912616106013	SIVA BHARATHI.P	III/ECE	1	1	1	1	,	1	1	,	1	1	10	P. Sathy
32	912616106014	SIVARUBINI.S	III/ECE	1	,	1	1	1	,	1	1	,	1	10	Siva
33	912616106015	THENMOZHI.A S	LEHARATHI	ENGIN	EERING	a	a	1	1	1	,	,	,	8	7/2

Kairkurchi - 622 303, Pudukkottai Dt.

34	912616106016	VINCY.A	III/ECE	1	,	,	1	1	,	,	1.	1	,	To	Vency &.
35	912616106302	SANKAVI M	III/ECE	1	1	1	1	,	1	,	,	1	,		
36	912615106001	AARTHI .M	IV/ECE	a	1	1	,	,	,	1	,	,	,	10	M. Santa
37	912615106002	ABIRAMI .C	IV/ECE	1	1	,	,	1	,	1	,	,	,	In	Abisami.e
38	912615106004	AKILA .S	IV/ECE	1	1	,	,	,	1	,	,	. /	,	10	AKIA.S
39	912615106005	ARTHI .M	IV/ECE	,	1	./	,	1	,	1	,	1	1	10	Aothi. A
40	912615106006	BAVADHARANI .M	IV/ECE	,	1	,	,	1	,	1	1.	1	,	10	Bendan
41	912615106007	DIVYABHARATHI .S	IV/ECE	,	1	,	,	1	,	- /	,	1	,	10	S. Day
42	912615106008	JAGADESWARI .K	IV/ECE	1	1	1	,	1	,	1	,	,	,		Fagadeshin
43	912615106009	MEENAKSHI .R	IV/ECE	,	,	,	,	1	,	a	a	1	,	10	Nechaking
44	912615106010	MEENAL .T	IV/ECE	,	1	,	1	1	,	,	,	1	,	10	1
45	912615106012	SARGUNAVALLI .C	IV/ECE	a	a	,	/	/	,	1	,	1	1	8	1. Mand
46	912615106013	THENMOZHI .K	IV/ECE	1	1	,	,	1	,	1	,	,		10	C Surgest
47	912615106014	VENNILA .K	IV/ECE	,	1	,	,	/	,	,	,	,	,	10	K. The sur
48	912615106301	MANIMEGALAI .S	IV/ECE	,	,	,	,	1	,	a		,	,	9	Hos
49	912615106701	SARADHA .S	IV/ECE	,	1	,	,	/	,	1	,	,	,	10	Carothan
50	912615106702	KAVIYA. S	IV/ECE	,	,	1	/	1	1	,	1	/	,	10	Skaniye

SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkottai Dt.

VAC Coordinator

HoD/ ECE HOD / ECE SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI.

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu - 622 303, India

Report on	Value	Added	Course

Title:

Digital System Design with Xilinx

Resource Person:

Mr.A.GANESAN Software Engineer. Maria Academy.

T. Nagar, Chennai 600059.

Date of conduct from:

18.06.2018

To: 22.06.2018 Duration:

30 Hours

Organized Department:

Electronics and Communication Engineering

Participant Year:

2/3/4

Semester:

ODD

No. of Students Registered:

Venue:

Seminar Hall, Ground Floor, SBECW

Outcome of Value Added Course (VAC): At the end of Course , Students can able to

- Design the system meeting the specifications
- Design the data path and the controller(s) to implement the functionality.
- Develop Verilog based programs and simulate digital circuits.
- Analyze a VHDL code and infer what circuit a synthesis tool might generate out of a code.
- Implement digital circuits in Xilinx FPGA processor using Hardware description Language experimentally.
- Design and code to exploit the architectural features of FPGA.

No. of students successfully completed the VAC course is 50 Students based on the following Assessment process.

Assessment Process

- Students securing more than 60% on total score and secured more than 75% in attendance is eligible to receive the certificate for the VAC course conducted
- Total Score = (0.5 *Attendance in VAC out of 100 percentage + 0.5 *Test mark in VAC out of 100 marks)

ordinator

HOD / ECE

SRI BHARATHI ENGINEERING

COLLEGE FOR WOMEN KAIKKURICHI,

PUDUKKOTTAI - 622 308

Dr. S.THILAGAVATHI M.E., Ph.D. PRINCIPAL

SRI BHARATHI ENGINEERING

COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ATCHAYA.G, III YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

GAR CHENNALGOODED TAME N

RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ABIRAMI.S, II YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from

18.06.2018 to 22.06.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph.D.

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

Ganesan RESOURCE PERSON



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. VENNILA .K, IV YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL
SRI BHARATHI ENGINEERING

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T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

Ganesan RESOURCE PERSON



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Nam	e of the Student :	Year/Sem:
AU F	Register Number:	
	Value Added Course on	"Digital System Design with Xilinx"
	MCQ QUEST	TIONS (25X1 = 25 Marks)
1.	Which of the following options con Electronics?	mes under the non – saturated logic family in Digital
	a) Emitter – coupled Logicb) High-Threshold Logic	c) Integrated – injection Logicd) Diode – Transistor Logic
2.	Which characteristic of IC in Digital particular transistor?	tal Circuits represents a function of the switching time of a
	a) Fan – out	c) Power dissipation
	b) Fan – in	d) Propagation delay
3.	Which gates in Digital Circuits are flop?	required to convert a NOR-based SR latch to an SR flip-
	a) Two 2 input AND gates	c) Two 2 input OR gates
	b) Two 3 input AND gates	d) Two 3 input OR gates
4.	What must be used along with synd	chronous control inputs to trigger a change in the flip flop?
	a) 0	c) Clock
	b) 1	d) Previous output
5.	What are the basic gates in MOS lo	ogic family?
	a) NAND and NOR	c) NAND and OR
	b) AND and OR	d) AND and NOR
6.	Which of the following is only pred	defined physical literal in VHDL?
	a) Voltage	c) Current
	b) Time	d) Distance
7.	Access types are similar to	in traditional programming languages.
	a) Pointers	c) Structures
	b) Arrays	d) Files
8.	Which of the following is default d	lelay in VHDL?
	a) Inertial delay	c) Delta delay
	b) Transport delay	d) Wire delay
9.	Transport delay is a kind of	Hand
	a) Synthesis delay	c) Inertial delay
	b) Simulation delayor. S.THILA	SAVATHI M.E., Ph. Wire delay

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input A changes after 10 ns	from 0 to 1 and it chan	as a delay of 20 nanosecond. If the value of ages again from 1 to 0 at 20 ns. At what
time, the value of output B	will be 1, if the transpo	
a) 20 ns		c) 40 ns
b) 30 ns		d) Output will remain zero
11. The process used for implen	nentation of sequential	logic in VHDL is called process.
a) Sequential process		c) Clocked process
b) Combinational process		d) Unlocked process
12. A user doesn't want to use to same by using any other key		tecting clock edge. It is possible to do the
a) True		b) False
13. PLA contains		
a) AND and OR arrays		c) NOT and AND arrays
b) NAND and OR arrays		d) NOR and OR arrays
o) with and one arrays		d) NOR and OR arrays
14. A PLA is similar to a ROM	in concept except that	as snown 3 langua or some dance.
 a) It hasn't capability to reac variables 	lonly	c) It doesn't provide full decoding to the
b) It hasn't capability to reac	d or write operation	d) It hasn't capability to write only
	equi l'entres eleccritair	
15. The complex programmable	logic device contains	several PLD blocks and
a) A language compiler		c) Global interconnection matrix
b) AND/OR arrays		d) Field-programmable switches
16. Which type of device FPGA	are?	
a) SLD		c) EPROM
b) SROM		d) PLD
E.JOHV.pillo		application amount of the solution of
17. In FPGA, vertical and horizon	ontal directions are sep	parated by
a) A line		c) A strobe
b) A channel		d) A flip-flop
18. In a digital clock application	n, the basic frequency	must be divided down as
a) 1 Hz		c) 100 Hz
b) 60 Hz	e with the manual of	d) 1000 Hz
		zaloh faltsonista
19. Which among the following circuit into a set of logic equ		rming design entry information of the
a) Simulation		c) Synthesis
b) Optimization		d) Verification S.THILAGAVATHI M.E., Ph.D.
		PRINCIPAL
		SRI BHARATHI ENGINEERING

COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Di



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edominantly associated with .
c) CPLDs
d) All of the above
he determination of resistance & capacitance of
c) Testing
d) Extraction
at gives the description of logic cells & their
c) Checklist
d) Dualist
are executed in physical design or layout synthesis circuit in target chip
onsible for converting an un optimized boolean
c) Optimization
d) All of the above
tools.
c) Both a and b
d) None of the above

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

Value Added Course on "Digital System Design with Xilinx"

MCQ ANSWER KEY

1	A	6	В	11	C	16	D	21	D
2	D	7	A	12	A	17	В	22	A
3	A	8	A	13	A	18	A	23	С
4	С	9	D	14	С	19	С	24	A
5	A	10	В	15	С	20	В	25	В

Dr. S.THILAGAVATHI M.E., Ph.D.

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Name of the Student: C. Kavya Year/Sem: 1 [1] AU Register Number: 912617106011 Value Added Course on "Digital System Design with Xilinx" MCQ QUESTIONS (25X1 = 25 Marks) Which of the following options comes under the non - saturated logic family in Digital Electronics? (a) Emitter – coupled Logic c) Integrated - injection Logic b) High-Threshold Logic d) Diode - Transistor Logic 2. Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor? a) Fan - out c) Power dissipation b) Fan - in (d) Propagation delay 3. Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flipflop? (a) Two 2 input AND gates c) Two 2 input OR gates b) Two 3 input AND gates d) Two 3 input OR gates 4. What must be used along with synchronous control inputs to trigger a change in the flip flop? a) 0 (c) Clock b) 1 d) Previous output 5. What are the basic gates in MOS logic family? (a) NAND and NOR c) NAND and OR b) AND and OR d) AND and NOR 6. Which of the following is only predefined physical literal in VHDL? a) Voltage c) Current (b) Time d) Distance 7. Access types are similar to ______ in traditional programming languages. (a) Pointers c) Structures b) Arrays d) Files 8. Which of the following is default delay in VHDL? a) Inertial delay c) Delta delay b) Transport delay d) Wire delay

Transport delay is a kind of

a) Synthesis delay

(b) Simulation delay

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c) Inertial delay Dr. S.THILAGAVATHI M.E. Ph.

d) Wire delay



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10. A buffer with single input A and single output B h	has a delay of 20 nanosecond. If the value of
input A changes after 10 ns from 0 to 1 and it chan	
time, the value of output B will be 1, if the transpo	
a) 20 ns	c) 40 ns
(b) 30 ns	d) Output will remain zero
11. The process used for implementation of sequential	l logic in VHDL is called process.
a) Sequential process	© Clocked process
b) Combinational process	d) Unlocked process
12. A user doesn't want to use the IF statement for de	etecting clock edge. It is possible to do the
same by using any other keyword in VHDL.	
a) True	b) False
13. PLA contains	
a) AND and OR arrays	c) NOT and AND arrays
b) NAND and OR arrays	d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except that	
a) It hasn't capability to read only	(c) It doesn't provide full decoding to the
variables	c) it doesn't provide fan decoding to the
b) It hasn't capability to read or write operation	d) It hasn't capability to write only
definition as the first of the first of standard the first field of the first	Lat What he made along with average with a so to
15 The complex programmable logic device contains	
a) A language compiler	© Global interconnection matrix
b) AND/OR arrays	d) Field-programmable switches
16. Which type of device FPGA are?	
a) SLD	a) EPROM
b) SROM	c) EPROM (d) PLD
b) Skow and the first state in the state ind	(a) PLD
17. In FPGA, vertical and horizontal directions are sep	parated by
a) A line	c) A strobe
(b) A channel	d) A flip-flop
18. In a digital clock application, the basic frequency	must be divided down as
a) 1 Hz	c) 100 Hz
b) 60 Hz	d) 1000 Hz
19. Which among the following is a process of transfo	orming design entry information of the
circuit into a set of logic equations?	acong. only morning or the
a) Simulation	© Synthesis
b) Optimization	d) Verification
Dr. S. I MILAGE ZATE	iva. E., Fil. D., and a manufactured ultra
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COLLEGE FOR WOMEN



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Name of the Student: A Dharant	ya Year/Sem: 11) / I
Name of the Student: A Dharant AU Register Number: 91261610	6005
	al System Design with Xilinx"
MCQ QUESTIONS	(25X1 = 25 Marks)
1. Which of the following options comes und	er the non – saturated logic family in Digital
Electronics?	22500rg Zaliptinghilling 2 (a)
(a) Emitter – coupled Logic	c) Integrated – injection Logic
b) High-Threshold Logic	d) Diode – Transistor Logic
particular transistor?	its represents a function of the switching time of a
a) Fan – out	c) Power dissipation
(b) Fan – in	Propagation delay
3. Which gates in Digital Circuits are required flop?	to convert a NOR-based SR latch to an SR flip-
(a) Two 2 input AND gates	c) Two 2 input OR gates
b) Two 3 input AND gates	d) Two 3 input OR gates
4. What must be used along with synchronous	s control inputs to trigger a change in the flip flop?
a) 0	© Clock
b) 1	d) Previous output
5. What are the basic gates in MOS logic fam a) NAND and NOR	ily?
	c) NAND and OR
(b) AND and OR	d) AND and NOR
6. Which of the following is only predefined p	physical literal in VHDL?
a) Voltage	c) Current
(b) Time	d) Distance
7. Access types are similar to in tr	aditional programming languages.
(a) Pointers	c) Structures
b) Arrays	d) Files
8. Which of the following is default delay in \	/HDL?
a) Inertial delay	c) Delta delay
(b) Transport delay	d) Wire delay
9. Transport delay is a kind of	Tenonical de la
a) Synthesis delay	c) Inertial delay Dr. S.THILAGAVATHI M.E.,Ph.I
b) Simulation delay	(d) Wire delay

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time, the value of output B will be 1, if the transpo	ort delay model is used?	
a) 20 ns	c) 40 ns	
(b) 30 ns	d) Output will remain zer	
1(Th	99400097	
M. The process used for implementation of sequential		process.
a) Sequential process	© Clocked process	
b) Combinational process	d) Unlocked process	
12. A user doesn't want to use the IF statement for de	tecting clock edge. It is nossi	ble to do the
same by using any other keyword in VHDL.	recting clock edge. It is possi	ble to do the
(a) True	b) False	
	o) i disc	
13. PLA contains		
a) AND and OR arrays	c) NOT and AND arrays	
b) NAND and OR arrays	d) NOR and OR arrays	
US O SAME STATE OF THE SAME ST	comession telephone as as as a second	
14. A PLA is similar to a ROM in concept except that	The state of the s	
 a) It hasn't capability to read only variables 	© It doesn't provide full of	lecoding to the
b) It hasn't capability to read or write operation	d) It hasn't capability to w	vrite only
15. The complex programmable logic device containsa) A language compilerb) AND/OR arrays	© Global interconnection d) Field-programmable sw	
IC WILL STORY		
16. Which type of device FPGA are?	PO BARCIA)	
a) SLD (b) SROM	c) EPROM	
U) SKOW	d) PLD	
17. In FPGA, vertical and horizontal directions are sep	parated by	
a) A line	c) A strobe	
(b) A channel	d) A flip-flop	
18. In a digital clock application, the basic frequency	must be divided down as	
(a) 1 Hz	c) 100 Hz	(4)
b) 60 Hz	d) 1000 Hz	
Application of the Control of the Co		
19. Which among the following is a process of transfo	rmina decian entry informati	on of the
circuit into a set of logic equations?	mining design entry informati	
a) Simulation	© Synthesis	Ma
	C) -,	
b) Optimization	d) VerificationS.THILA	GAVATHI ME.,P

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20. An Antifuse programming technology is pr	redominantly associated with
a) SPLDs	c) CPLDs
(b) FPGAs	d) All of the above
21. In VLSI design, which process deals with t	he determination of resistance & capacitance of
interconnections?	
a) Floor planning	c) Testing
b) Placement & Routing	(d) Extraction
22 1	
22. In logic synthesis, is an EDIF that inter connections.	at gives the description of logic cells & their
(a) Netlist	a) Charliff
b) Shitlist	c) Checklist d) Dualist
1	d) Dualist
23. Which among the following operation/s is/a	are executed in physical design or layout synthesis
stage?	
a) Placement of logic functions in optimized	circuit in target chip
b) Interconnection of components in the chip	p
c) Both a and bd) None of the above	
d) None of the above	
24. In synthesis flow, which stage/s is/are resp	onsible for converting an un optimized boolean
description to PLA format?	consiste for converting an un optimized boolean
(a) Flattening	c) Optimization
b) Translation	d) All of the above
	d) All of the above
25. In floorplanning, placement and routing are	tools.
a) Front end	c) Both a and b
b)Back end	d) None of the above
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Dr. S.THILAGAV	ATHIME PhD
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Name of the Student : T. MEENAL	Year/Sem: IV VII
AU Register Number: 912615106	010
Value Added Course on "Digit	al System Design with Xilinx"
MCQ QUESTIONS	5(25X1 = 25 Marks)
Which of the following options comes und Electronics?	er the non - saturated logic family in Digital
a Emitter – coupled Logic	c) Integrated – injection Logic
b) High-Threshold Logic	d) Diode – Transistor Logic
particular transistor?	uits represents a function of the switching time of a
a) Fan – out	c) Power dissipation
b) Fan – in	(d) Propagation delay
Which gates in Digital Circuits are required flop?	d to convert a NOR-based SR latch to an SR flip-
(a) Two 2 input AND gates	c) Two 2 input OR gates
b) Two 3 input AND gates	d) Two 3 input OR gates
What must be used along with synchronous a) 0	s control inputs to trigger a change in the flip flop?
b) 1	d) Previous output
5. What are the basic gates in MOS logic fam	ily?
(a) NAND and NOR	c) NAND and OR
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6. Which of the following is only predefined p	physical literal in VHDL?
a) Voltage	c) Current
(b) Time	d) Distance
7. Access types are similar to in tr	aditional programming languages.
(a) Pointers	c) Structures
b) Arrays	d) Files
8. Which of the following is default delay in V	/HDL?
(a) Inertial delay	c) Delta delay
b) Transport delay	d) Wire delay
9. Transport delay is a kind of	
a) Synthesis delay	c) Inertial delayr. S.THILAGAVATHI M.E., Ph.D.
b) Simulation delay	SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN
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time, the value of output B will be 1, if the transpo	
a) 20 ns	c) 40 ns
(b) 30 ns	d) Output will remain zero
11. The process used for implementation of sequentia a) Sequential process	l logic in VHDL is called process.
a) Sequential process	c) Clocked process
b) Combinational process	d Unlocked process
12. A user doesn't want to use the IF statement for de same by using any other keyword in VHDL.	etecting clock edge. It is possible to do the
a) True	b False
13. PLA contains	
(a) AND and OR arrays	c) NOT and AND arrays
b) NAND and OR arrays	d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except that	30) Which cans in Duited Circuit un Roma
a) It hasn't capability to read only variables	© It doesn't provide full decoding to the
b) It hasn't capability to read or write operation	d) It hasn't capability to write only
polytorijas central intens to trigger a charge in the Hip flag	
15. The complex programmable logic device contains	^
a) A language compiler	(c) Global interconnection matrix
b) AND/OR arrays	d) Field-programmable switches
16. Which type of device FPGA are?	
a) SLD	c) EPROM
b) SROM	(d) PLD
17. In FPGA, vertical and horizontal directions are se	parated by
a) A line	c) A strobe
(b) A channel	d) A flip-flop
18. In a digital clock application, the basic frequency	must be divided down as
(a) 1 Hz	c) 100 Hz
	d) 1000 Hz
b) 60 Hz	
	valohtnisenidal
b) 60 Hz 19. Which among the following is a process of transfer	orming design entry information of the
b) 60 Hz 19. Which among the following is a process of transfer circuit into a set of logic equations? a) Simulation	© Synthesis
b) 60 Hz 19. Which among the following is a process of transfer circuit into a set of logic equations?	© Synthesis

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a) SPLDs	ology is predominantly associated with c) CPLDs
(b) FPGAs	d) All of the above
interconnections?	eals with the determination of resistance & capacitance of
a) Floor planningb) Placement & Routing	c) Testing (d) Extraction
22. In logic synthesis, is an inter connections.	EDIF that gives the description of logic cells & their
a) Netlist b) Shitlist	C Checklist d) Dualist
23. Which among the following operastage? a) Placement of logic functions in b) Interconnection of components c) Both a and b d) None of the above	
24. In synthesis flow, which stage/s idescription to PLA format?	is/are responsible for converting an un optimized boolean
a) Flatteningb) Translation	d) All of the above
25. In floorplanning, placement and ro	outing are tools.
a) Front end	c) Both a and b
Back end	d) None of the above
SRIBHA	AGAVATHI M.E., Ph.D., PRINCIPAL RATHI ENGINEERING EGE FOR WOMEN 1-622 303, Pudukkottai Dt.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONENGINEERING

ACADEMIC YEAR ODD SEMESTER (2018-2019)

MARK SHEET FOR VALUE ADDED COURSE- "DIGITAL SYSTEM DESIGN WITH XILINX"

24	REGISTER	NAME	YEAR	Attendance (A)		VAC -MCQ TEST (B)		OVERALL MARK(100)
S.NO	NUMBER		& BRANCH	No.of Sessions Attented	Marks (100)	No.of Correct Answer	Marks (100)	(50% of A + 50% of B)
1	912617106001	ABIRAMI.S	II /ECE	10	100	22	88	94
2	912617106002	ABISHEKA.S	II /ECE	10	100	23	92	96
3	912617106003	ATSHAYA.R	II /ECE	9	90	21	84	87
4	912617106004	BAVADHARANI.A	II /ECE	9	90	20	80	85
5	912617106005	BHUVANESHWARI.B	II /ECE	10	100	19	76	88
6	912617106006	DHIVYA.L	II /ECE	10	100	20	80	90
. 7	912617106007	GOWSALYA.D	II /ECE	10	100	21	84	92
8	912617106009	INDHUMATHI.S	II /ECE	9	90	19	76	83
9	912617106010	KANIMOZHI.D	II /ECE	10	100	18	72	86
10	912617106011	KAVYA.C	II /ECE	10	100	22	88	94
11	912617106012	KEERTHANA.G	II /ECE	10	100	20	80	90

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	012617106012	MALIECHWADI C			T			
12	912617106013	MAHESHWARI.G	II /ECE	10	100	19	76	88
13	912617106014	MANOHARI.M	II /ECE	10	100	18	72	86
14	912617106015	MARAGATHALAKSHMI.S	II /ECE	8	80	20	80	80
15	912617106017	SAFRIN NISHA.S	II /ECE	10	100	20	80	90
16	912617106018	SUBASHINI.M	II /ECE	10	100	18	72	86
17	912617106019	SUBASHINI.T	II /ECE	8	80	19	76	78
18	912617106020	VINTHIYA.R	II /ECE	10	100	22	88	94
19	912616106001	ABINAYA.R	III /ECE	10	100	19	76	88
20	912616106002	AGALYA.A	III /ECE	8	80	18	72	76
21	912616106003	ATCHAYA.G	III /ECE	10	100	19	76	88
22	912616106004	DEEPA.N	III /ECE	10	100	22	88	94
23	912616106005	DHARANIYA.A	III /ECE	9	90	18	72	81
24	912616106006	JEEVITHA.U	III /ECE	10	100	19	76	88
25	912616106007	MAHESWARI.V	III /ECE	8	80	21	84	82
26	912616106008	PAZHANIYAMMAL.R	III /ECE	10	100	23	92	96
27	912616106009	PRIYANKA.E	III /ECE	10	100	21	84	92
28	912616106010	ROJA.A	III /ECE	10	100	23	92	96
29	912616106011	SHANMUGAPRIYA.R	III /ECE	10	100	19	76	88
30	912616106012	SHIYAMALA.E	III /ECE	10	100	19	76	88
31	912616106013	SIVA BHARATHI.P	III /ECE	10	100	18	72	86
32	912616106014	SIVARUBINI.S	III /ECE	10	100	23	82	91

Dr S.THILAGAVATHI M.E., Ph.D.,
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33	912616106015	THENMOZHI.A	III /ECE	8	80	18	72	76
34	912616106016	VINCY.A	III /ECE	10	100	18	72	86
35	912616106302	SANKAVI M	III /ECE	10	100	19	76	88
36	912615106001	AARTHI .M	IV/ECE	9	90	18	72	81
37	912615106002	ABIRAMI .C	IV/ECE	10	100	20	80	90
38	912615106004	AKILA .S	IV/ECE	10	100	19	76	88
39	912615106005	ARTHI .M	IV/ECE	10	100	18	72	86
40	912615106006	BAVADHARANI .M	IV/ECE	10	100	18	72	86
41	912615106007	DIVYABHARATHI .S	IV/ECE	10	100	19	76	88
42	912615106008	JAGADESWARI .K	IV/ECE	10	100	17	68	84
43	912615106009	MEENAKSHI .R	IV/ECE	8	80	19	76	78
44	912615106010	MEENAL .T	IV/ECE	10	100	21	84	92
45	912615106012	SARGUNAVALLI.C	IV/ECE	8	80	20	80	80
46	912615106013	THENMOZHI .K	IV/ECE	10	100	15	60	80
47	912615106014	VENNILA .K	IV/ECE	10	100	22	88	94
48	912615106301	MANIMEGALAI .S	IV/ECE	9	90	19	76	83
49	912615106701	SARADHA .S	IVÆCE	10	100	23	92	96
50	912615106702	KAVIYA. S	IV/ECE"	. 10	100	20	80	90

VAC Coordinator

Dr. S.THILAGAVATHI M.E., Ph.D.,
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HOD / ECE SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI, PUDUKKOTTAI - 622 303



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING ACADEMIC YEAR 2018-2019/EVEN SEMESTER

DEPARTMENT CIRCULAR

Value Added Course offered by the Department of ECE will be conducted for all Second, Third and Final year students on "Antenna Design using High Frequency Simulation Software" in association with Maria Academy from 10.12.2018 to 14.12.2018. Certificates will be issued to the eligible participants at the end of the

S.No	Name of the Course	Resource Person
1	Antenna Design using High Frequency Simulation Software	Er.A.GANESAN, Software Engineer, Maria Academy, No 58, 17, S Usman Road, Near Bus stand, Kannammapet, T. Nagar, Chennai 600 059. Tamil Nadu . Mail.Id:mariatrainingacademy@gmail.com

Cc:

course.

- Principal Office
- IQAC Coordinator
- Class In charges- II, III &IV Year
- II ,III & IV Year ECE Students
- Notice Board

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KAIKKURICHI,
PUDUKKOTTAI - 622 303

Date: 03.12.2018

Dr. S.THILAGAVATHIM.E.,Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING <u>ACADEMIC YEAR 2018-2019/EVEN SEMESTER</u>

Value Added Course on "Antenna Design Using High Frequency Simulation Software"

SYLLABUS

S.NO	TOPIC COVERED	DURATION (in hours)	DATE
1	Introduction to the course and high-frequency simulation software. Review of antenna fundamentals and electromagnetic theory.	2	10.12.2018
2	Overview of various types of antennas and their applications. Introduction to the chosen simulation software and its interface.	1	10.12.2018
3	Modeling simple wire antennas (dipole, monopole) using the simulation software.Radiation pattern analysis and gain calculations.	3	10.12.2018
4	Design and simulation of patch antennas. Understanding bandwidth, polarization, and impedance matching. Simulation of array antennas (linear and planar arrays).	3	11.12.2018
5	Beamforming techniques and phased arrays.	3	11.12.2018
6 -	Introduction to microstrip antennas and their design using the software.	3	12.12.2018
7	Design and simulation of helical antennas. Circularly polarized antennas and axial ratio.	3	12.12.2018
8	Optimization algorithms for antenna design.	3	13.12.2018
9	Design and simulation of Yagi-Uda antennas and log- periodic antennas.	3	13.12.2018
10	Antenna arrays with non-uniform excitation.	3	14.12.2018
11	Introduction to antenna measurement techniques and validation of simulation results. Understanding measurement errors and calibration.	3	14.12.2018
	Total Hours	3	0

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Dr. S.THILAGAVATHI M.E., Ph.D.)
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DEPARTMENT OF ELECTRONICS AN COMMUNICATIONENGINEERING ACADEMIC YEAR EVEN SEMESTER (2018-2019)

STUDENT PARTICIPATION LIST FOR VALUE ADDED PROGRAM

Antenna Design Using High Frequency Simulation Software

S.NO	REG.NO	NAME	YEAR & BRANCH
1	912617106001	ABIRAMI.S	II & ECE
2	912617106002	ABISHEKA.S	II & ECE
3	912617106003	ATSHAYA.R	II & ECE
4	912617106004	BAVADHARANI.A	II & ECE
5	912617106005	BHUVANESHWARI.B	II & ECE
6	912617106006	DHIVYA.L	II & ECE
7	912617106007	GOWSALYA.D	II & ECE
8	912617106009	INDHUMATHI.S	II & ECE
9	912617106010	KANIMOZHI.D	II & ECE
10	912617106011	KAVYA.C	II & ECE
11	912617106012	KEERTHANA.G	II & ECE
12	912617106013	MAHESHWARI.G	II & ECE
13	912617106014	MANOHARI.M	II & ECE
14	912617106015	MARAGATHALAKSHMI.S	II & ECE
15	912617106017	SAFRIN NISHA.S	II & ECE
16	912617106018	SUBASHINI.M	II & ECE
17	912617106019	SUBASHINI.T	II & ECE
18	912617106020	VINTHIYA.R	II & ECE
19	912616106001	ABINAYA.R	III & ECE
20	912616106002	AGALYA.A	III & ECE
21	912616106003	ATCHAYA.G	III & ECE
22	912616106004	DEEPA.N	III & ECE
23	912616106005	DHARANIYA.A	III & ECE
24	912616106006	JEEVITHA,U	III & ECE
25	912616106007	MAHESWARI	III & ECE

PRINCIPAL SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303 Pudukketta De

S.NO	REG.NO	NAME	YEAR & BRANCH III & ECE		
26	912616106008	PAZHANIYAMMAL.R			
27	912616106009	PRIYANKA.E	III & ECE		
28	912616106010	ROJA.A	III & ECE		
29	912616106011	SHANMUGAPRIYA.R	III & ECE		
30	912616106012	SHIYAMALA.E	III & ECE		
31	912616106013	SIVA BHARATHI.P	III & ECE		
32	912616106014	SIVARUBINI.S	III & ECE		
33	912616106015	THENMOZHI.A	III & ECE		
34	912616106016	VINCY.A	III & ECE		
35	912616106302	SANKAVI M	III & ECE		
36	912615106001	AARTHI .M	IV & ECE		
37	912615106002	ABIRAMI .C	IV & ECE		
38 .	912615106004	AKILA .S	IV & ECE		
39	912615106005	ARTHI .M	IV & ECE		
40	912615106006	BAVADHARANI .M	IV & ECE		
41	912615106007	DIVYABHARATHI .S	IV & ECE		
42	912615106008	JAGADESWARI .K	IV & ECE		
43	912615106009	MEENAKSHI .R	IV & ECE		
44	912615106010	MEENAL .T	IV & ECE		
45	912615106012	SARGUNAVALLI.C	IV & ECE		
46	912615106013	THENMOZHI .K	IV & ECE		
47	912615106014	VENNILA .K	IV & ECE		
48	912615106301	MANIMEGALAI .S	IV & ECE		
49	912615106701	SARADHA .S	IV & ECE		
50	912615106702	KAVIYA. S	IV & ECE		

VAC Coordinator

HoD/ECE HOD / ECE

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI,

PUDUKKOTTAI - 622 303.

Dr. S.THILAGAVATHI M.E., Ph.D.

PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25)
KAIKKURICHI, PUDUKKOTTAI-622 303
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
ACADEMIC YEAR EVEN SEMESTER (2018-2019)

<u>ATTENDANCE SHEET FOR VALUE ADDED COURSE- ANTENNA DESIGN USING HIGH FREQUENCY SIMULATION SOFTWARE</u>

.NO	REG. NO	NAME	YEAR/	10.12.2018		11.12.2018		12.12.2018		13.12.2018		14.12.2018		NO. OF	SIGN OF
	REG. NO	NAME	BRANCH	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	SESSIONS ATTENDED	STUDENT
1	912617106001	ABIRAMI.S	II /ECE	1	1	1	1	1	1	1	1	1	1	10	S. Abirami
2	912617106002	ABISHEKA.S	II /ECE	1	1	,	1	,	1	1	1	1	1	lo	S. Dha
3	912617106003	ATSHAYA.R	II /ECE	1	1	a	a	1	,	1	1	1	1	8	R. Atal
4	912617106004	BAVADHARANI.A	II /ECE	1	1	1	1	1	1	1	1	,	1	10	D. Baradhen
5	912617106005	BHUVANESHWARI.B	II /ECE	a	a	./	1	1	1	1	,	/	1	8	B-Bhuranesh
6	912617106006	DHIVYA.L	II /ECE	1	1	,	,	,	1	a	1	,	1	9	L. Divy
7	912617106007	GOWSALYA.D	II /ECE	1	1	,	,	,	1	1	1	,	1	10	D Course
8	912617106009	INDHUMATHI.S	II /ECE	a	,	1	1	1	1	,	1	,	1	10	S. Indhumath
9	912617106010	KANIMOZHI.D	II /ECE	a	1	,	1	1	1	1	,	,	,	9	D. Kanings
10	912617106011	KAVYA.C	II /ECE	1	1	1	1	,	1	1	1	1	1	10	C. Karya
11	912617106012	KEERTHANA.G	II /ECE	1	1	,	,	,	1	, ,	,	,	,	10	a. Keethan
9	912617106010 912617106011	KANIMOZHI.D KAVYA.C	II /ECE		1	1 1 1	1 1 1	1 1	1	/	1 1 1 1	1 1	1 1 1	9 9 10	

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PRINCIPAL
SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN

12	912617106013	MAHESHWARI.G	II /ECE	1	1	1	1	,	1	1	1	1	1	10	(y. Mahemari
13 ·	912617106014	MANOHARI.M	II /ECE	1	1	1	1	,	,	1	1	1	,	10	M. Mari
14	912617106015	MARAGATHA LAKSHMI.S	II /ECE	1	1	1	1	a	,	1	,	1	,	9	S. Marazatralus
15	912617106017	SAFRIN NISHA.S	II /ECE	1	,	1	1	1	1	1	,	1	1	10	S. Saferin Nisk
16	912617106018	SUBASHINI.M	II /ECE	1	,	,	,	1	,	,	1	,	1	10	M. Subashini
17	912617106019	SUBASHINI.T	II /ECE	,	,	/	1	1	,	1	1	,	1	10	J. Sului.
18	912617106020	VINTHIYA.R	II /ECE	,	1	1	1	1	,	1	,	1	. /	10	R. Vinthing
19	912616106001	ABINAYA.R	III/ECE	1	1	1	1	,	,	,	,	1	,	10	R. Abinaya
20	912616106002	AGALYA.A	III/ECE	1	1	1	1	1	,	1	1	1	1	10	t. Agalya
21	912616106003	ATCHAYA.G	III/ECE	1	1	1	1	,	,	1	1	1	,	10	G. Atchase
22	912616106004	DEEPA.N	III/ECE	1	1	1	1	1	1	1	,	1	1	10	N. Peele
23	912616106005	DHARANIYA.A	III/ECE	1	1	1	1	1	1	1	1	1	1	10	D. Dherry
24	912616106006	JEEVITHA.U	III/ECE	1	,	1	,	1	,	,	,	,	,	10	V. Feerita
25	912616106007	MAHESWARI.V	III/ECE	1	1	1	1	a	a	1	.1	,	1	8	V. Malieni
26	912616106008	PAZHANIYAMMAL.R	III/ECE	1	,	1	1	1	1	1	,	,	,	10	Parter
27	912616106009	PRIYANKA.E	III/ECE	,	1	1	1	,	1	1	.,	1	,	10	Porganta E
28	912616106010	ROJA.A	III/ECE	1	1	1	1	1	1	1	1	1	,	10	Pote.
29	912616106011	SHANMUGAPRIYA.R	III/ECE	,	,	1	1	,	. /	,	,	/	,	10	Shanpenya
30	912616106012	SHIYAMALA.E	III/ECE	1	,	1	1	/	1	,	/	1	1	10	6 South
31	912616106013	SIVA BHARATHI.P	III/ECE	,	,	,	,	,	,	.,	,	,	,	10	P. Salline

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303 Pudukhatta Da

32	912616106014	SIVARUBINI.S	III/ECE	1	/	/	1	1	/	,	/	/	1	10	Swz.
33	912616106015	THENMOZHI.A	III/ECE	1	/	1	1	1	,	1	1	1	1	10	The
34	912616106016	VINCY.A	III/ECE	1	1	1	1	1	1	1	1	1	,	10	Vency &
35	912616106302	SANKAVI M	III/ECE	1	1	1	,	1	,	1	1	1	1	10	M. Santan
36	912615106001	AARTHI .M	IV/ECE	a	. /	1	1	1	1	1	1	1	1	9	M. daethi
37	912615106002	ABIRAMI .C	IV/ECE	1	1	1	1	1	,	1	1	1	,	10	Abirami.c
38	912615106004	AKILA .S	IV/ECE	1	1	1	1	,	/	1	/	1	,	10	Akila-S
39	912615106005	ARTHI .M	IV/ECE	1	1	/	1	1	1	,	1	1	,	10	Aothi N
40	912615106006	BAVADHARANI .M	IV/ECE	1	1	1	/	1	1	1	1	,	1	10	Baraton
41	912615106007	DIVYABHARATHI .S	IV/ECE	1	1	1	1	1	/	a	1	,	,	9	Q. Olingan
42	912615106008	JAGADESWARI .K	IV/ECE	1	1	/	1	1	1	1	1	1	1	10	Faga descri
43	912615106009	MEENAKSHI .R	IV/ECE	1	1	1	1	1	/	,	1	1	1	10	Maeraken
44	912615106010	MEENAL .T	IV/ECE	1	1	1	1	1	/	1	1	1	1	10	T. Meend
45	912615106012	SARGUNAVALLI.C	IV/ECE	1	/	1	1	1	/	1	,	/	,	10	C. Surgnob!
46	912615106013	THENMOZHI .K	IV/ECE	1	1	/	1	a	a	1	1	,	,	8	K. Than
47	912615106014	VENNILA .K	IV/ECE	1	1	1	1	1	1	,	,	,	/	10	Ventina
48	912615106301	MANIMEGALAI .S	IV/ECE	a	1	1	1	1	,	1	/	,	1	9	ten
49	912615106701	SARADHA .S	IV/ECE	1	1	1	1	1	1	,	1	1	1	10	Samous
50	912615106702	KAVIYA. S	IV/ECE	1	1	1	1	1	1	1	1	1	,	10	B. Kariya
								*							The state of the s

VAC Coordinator

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. HoD/ECE HOD / ECE SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI, PUDUKKOTTAI - 622 308.

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Report on Value Added Course

Title:

Antenna Design using High Frequency Simulation Software

Resource Person:

Mr.A.GANESAN Software Engineer, Maria Academy,

T. Nagar, Chennai 600059.

Date of conduct from:

10.12.2018

To: 14.12.2018

Duration:

30 Hours

Organized Department:

Electronics and Communication Engineering

Participant Year:

2/3/4

Semester: EVEN

No. of Students Registered:

50

Venue: §

Seminar Hall, ,Ground Floor, SBECW

Outcome of Value Added Course (VAC) : At the end of Course , Students can able to

- Design and or develop a prototype in the area of passive/Active circuits/Antennas.
- Design and analyze various antennas.
- Develops an idea to compare the performance of different types of antennas.
- Develops an insight to optimize different performance parameters of antenna to have more advance performance.
- Creates an interest to design a new form of antenna which can be implemented in specific wireless applications.
- Design and analysis of Microwave Antennas Using HFSS.

No. of students successfully completed the VAC course is <u>50 Students</u> based on the following Assessment process.

Assessment Process

- Students securing more than 60% on total score and secured more than 75% in attendance is eligible to receive the certificate for the VAC course conducted
- Total Score = (0.5 *Attendance in VAC out of 100 percentage + 0.5 *Test mark in VAC out of 100 marks)

VAC Coordinator

HoD ECE

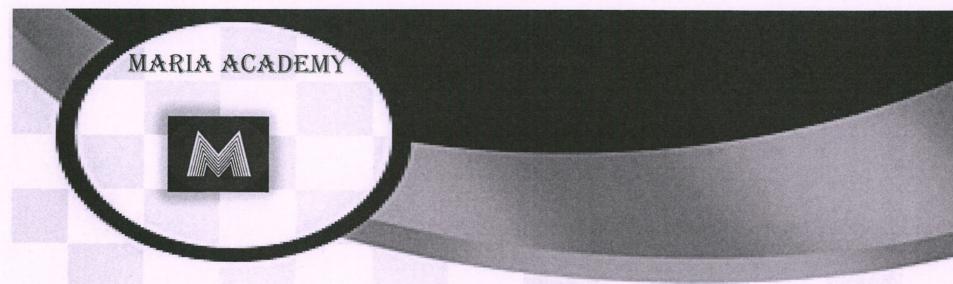
HOD / ECE

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI, PUDUKKOTTAI - 622 303

r. S.THILAGAVATHI M.E.,Ph.I. PRINCIPAL

Principal

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



CERTIFICATE OF PARTICIPATION

This certificate recognizes that Ms. BAVADHARANI.A, II YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Antenna Design Using High Frequency Simulation Software Conducted from 10.12.2018 to 14.12.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. Ganesan RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. DEEPA.N, III YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Antenna Design High Frequency Simulation Software Conducted from 10.12.2018 to 14.12.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph. B.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. Ganesan RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM



CERTIFICATE OF PARTICIPATION

This certificate recognizes that Ms. MEENAL .T, IV YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Antenna Design Using High Frequency Simulation Software Conducted from 10.12.2018 to 14.12.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHIM.E.,Ph.D.,

SRI BHARATHI ENGINEERING **COLLEGE FOR WOMEN**

Kaikkurchi - 622 303, Pudukkotiai Dt. T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

RESOURCE PERSON



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India

Name of the Student	Name	of	the	Stu	den	t	:
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Year/Sem:

AU Register Number:

Value Added Course on "Antenna Design using HFSS"

\underline{MCQ} QUESTIONS (20X1 = 20 Marks)

1. EIRP in an isotropic antenna stands for	2. An example of each law polarization is a polarization of a 100
a)Effective isotropic radiated power b)Equivalent isotropic radiation power	c)Entropic isotropic radiated power d)Equivalent isolated radiated power
2. What is the gain factor (in dB) of an iso a)1b)0	tropic radiator in all directions? c)Infinity d)0db
3. What is the gain factor of an isotropic raa) 1b)0	adiator in all directions? c)Infinity d)0db
4. What is the shape of isotropic radiation	when observed in 3D?
a)Doughnut shaped b)Spherical	c)Figure of Eight d)Circle
Isotropic radiation is also known as a)Omni-directional radiation b)Bi-directional radiation	c)Tri- directional radiation d)None of the above
6. The characteristics of an antenna's radia ways.a)2 b)3 c)4	tion pattern can be represented in number of d)4
7. Transmitting antenna has which of the fa a)Side lobes are low b)Efficiency is high	ollowing parameter as a basic requirement. c)High SNR value d)High SNR value
8. Which of the following is an equation for a)ERP(dBW) = EIRP (dBW) - 2.15dBi b)ERP(dBW) = EIRP (dBW) - 3.15dBi	c)ERP(dBW) = EIRP (dBW) + 2.15 dBi
9.Radiation patterns can be represented in a)Field patterns b)Power patterns	c)Both a and b d)Direction pattern

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10.A 2-D radiation pattern graph contains how mar a)2 b)3 c)5	ny coordinates?
11. Antenna can be polarized in ways.	
a)3 b)2 c)5	d)1
12. An example of circular polarization is	
a)GPS	c)TV signals
b)Radio wave	d)Mobile communication signals
13. Which of the following is the frequency of hori	zontal polarization?
a)1 GHz	c)15 GHz
b)10 GHz	d)20 GHz
14. Magnetic field in EM wave is plotted on	axis.
a) X-axis	c)Z-axis
b) Y-axis	d)Either a or b
15. Units of Poynting vector is	
a)W/m2 b)W/m \overline{c})m/W	d)wm
16. If the wavelength is bigger than the length of didipole.	
a)Infinitesimal dipole	c)Short dipole
b)Long dipole	d)Any of the above
17. What is the range of frequency in a V-shaped at	
a)33KHz to 300 GHz	c) 30 MHz to 300 GHz
b)3 to 30 MHz	d)31KHz to 300 GHz
	- 10 Ed Sin
18. What is the beam width for a half wave dipole	
a) 90°	c) 50°
b) 180°	d) 250°
19. What is the impedance of the folded dipole anto	enna?
a) 50Ω	c) 300Ω
b) 100Ω	d) 20Ω
20. Which of the following antennas produce a ver	tical radiation pattern?
a) Dipole antenna	c) Marconi antenna
b) Yagi antenna	d) Hertz antenna
A COLETHII AGAVATHI M.E.,	
PRINCIPAL PRINCIPAL	NG MEALINY, 2 HO
Kaikkurchi - 622 303, Pudukkotia	SRIBHARATHI Je.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/EVEN SEMESTER

Value Added Course on "Antenna Design Using High Frequency Simulation Software"

MCQ ANSWER KEY

1	A	6	В	11	В	16	A
2	D	7	В	12	A	17	В
3	A	8	A	13	A	18	A
4	A	9	С	14	В	19	C
5	A	10	A	15	A	20	С

Dr. S.THILAGAVATHI M.E.C.Ph.D.,

PRINCIPAL SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

Kaikkurchi - 622 303, Pudukkottai Dt.



Year/Sem: II/V

COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu – 622 303, India Name of the Student: P. Atshaya

AU Register Number: 91261	7106003
	"Antenna Design using HFSS"
MCQ QUESTIC	ONS (20X1 = 20 Marks)
	1 90 1
1 EIRP in an isotropic antenna stands for _	
(a) Effective isotropic radiated power b) Equivalent isotropic radiation power	c)Entropic isotropic radiated power d)Equivalent isolated radiated power
2. What is the gain factor (in dB) of an isotr a)1 b)0	copic radiator in all directions? c)Infinity d)0db
3. What is the gain factor of an isotropic rad a)1 b)0	liator in all directions? c)Infinity d)0db
4. What is the shape of isotropic radiation w	when observed in 3D?
a)Doughnut shaped b)Spherical	©Figure of Eight d)Circle
5. Isotropic radiation is also known as	bil ong tipole
a)Omni-directional radiation b)Bi-directional radiation	c)Tri- directional radiation d)None of the above
6. The characteristics of an antenna's radiation	on pattern can be represented in number of
ways. a)2 b)3 c)4	d)4
7. Transmitting antenna has which of the fol a)Side lobes are low	lowing parameter as a basic requirement. c)High SNR value
(b) Efficiency is high	d)High SNR value
8. Which of the following is an equation for a)ERP(dBW) = EIRP (dBW) - 2.15dBi b)ERP(dBW) = EIRP (dBW) - 3.15dBi	ERP of an isotropic antenna? c)ERP(dBW) = EIRP (dBW) + 2.15dBi d)ERP(dBW) = EIRP (dBW) * 2.15dBi
9.Radiation patterns can be represented in te	erms of types.
(a)Field patterns	c)Both a and b
b)Power patterns	d)Direction pattern
SRI BHARRYHERMONGER	Dr. S.THILAGAVATHI M.E.,Ph.D., PRINCIPAL SRI BHARATHI ENGINEERING



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10.A 2-D radiation p	attern graph contains how m	any coordinates?
(a)2 b).		d)1
Cean	Suren uffestel med sons	THE COLUMN DAYS OF THE PARTY OF
11. Antenna can be p	oolarized in way	S.
(b)2	c)5	d)1
	rcular polarization is	· saladanta constan internativo di 1915. I
		, ,
b)Radio wave		d)Mobile communication signals
12 Which of the fall	assing is the freezeway of he	risental relevization?
	lowing is the frequency of no	
0		
b) to Gnz		u)20 GHZ
14 Magnetic field in	EM wave is plotted on	axis
(b) I unis		a)Billiot a of o
15. Units of Poynting	g vector is .	
		d)wm
	n is bigger than the length of	dipole then it is termed as a type of
	at a Control	hispharical
	pole	
b)Long dipole		d)Any of the above
17 AVI -4 :- 4b	- 66	mounted and the country of the count
· ·		
	GHZ	
(b)3 to 30 MHZ		d)31KHZ to 300 GHZ
18 What is the hean	width for a half wave dipol	e antenna?
	width for a harr wave dipor	
0) 100		Will STE RESULT SOURTH
19. What is the impe	edance of the folded dipole ar	ntenna?
		d) 20Ω
Selection 14		TORREST - LANGUE AND - CARDINATION
20. Which of the fol	lowing antennas produce a v	ertical radiation pattern?
11. Antenna can be polarized in	(c) Marconi antenna	
b) Yagi antenna		d) Hertz antenna
C-V X	to the whole	
		Dr. S. THU ACCUMENT
		PRINCE Ph D
		SRI BHARATHI ENGINEEDING
		MAIHIENGINEED

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b)Power patterns

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Name of the Student: A RoJA	Year/Sem: III / VI
AU Register Number: 912616	106010
Value Added Course on	"Antenna Design using HFSS"
AU Register Number: 9126166000 Value Added Course on "Antenna Design using HFSS" MCO QUESTIONS (20X1 = 20 Marks) 1. EIRP in an isotropic antenna stands for	$\frac{\text{ONS (20X1 = 20 Marks)}}{20}$
1. EIRP in an isotropic antenna stands for _	A POXIMINE OF LEVELEY COLUMN CONTRACTOR OF
a Effective isotropic radiated power b) Equivalent isotropic radiation power	c)Entropic isotropic radiated power d)Equivalent isolated radiated power
/a)1	c)Infinity
(a) 1	c)Infinity
4. What is the shape of isotropic radiation w	hen observed in 3D?
5. Isotropic radiation is also known as	along and the
ways.	on pattern can be represented in number of
a)2 (b)3 c)4	d)4
a)Side lobes are low	c)High SNR value
2000	And the appropriate the constant of the consta
(a) $ERP(dBW) = EIRP(dBW) - 2.15dBi$	c)ERP(dBW) = EIRP (dBW) + 2.15 dBi
9.Radiation patterns can be represented in ter	

d)Direction pattern

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL
SRI BHARATHI ENGINEERING

COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkotiai Dt.



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10.A 2-D radiation pattern graph contains b)3 c)5	s how many coordinates? d)1
a)3 b)2 c)5	ways.
12. An example of circular polarization is	c)TV signals
b)Radio wave	d)Mobile communication signals
13. Which of the following is the frequency	cy of horizontal polarization?
b)10 GHz	c)15 GHz d)20 GHz
14. Magnetic field in EM wave is plotted	
a) X-axis b) Y-axis	c)Z-axis d)Either a or b
15. Units of Poynting vector is c)m/W	d)wm
16. If the wavelength is bigger than the le dipole.	ength of dipole then it is termed as a type of
(a)Infinitesimal dipole	c)Short dipole
b)Long dipole	d)Any of the above
17. What is the range of frequency in a V	
a)33KHz to 300 GHz	c) 30 MHz to 300 GHz
(b)3 to 30 MHz	d)31KHz to 300 GHz
18. What is the beam width for a half way	ve dinole antenna?
a) 90°	c) 50°
b) 180°	d) 250°
19. What is the impedance of the folded of	dipole antenna?
a) 50Ω	② 300Ω
b) 100Ω	d) 20Ω
20. Which of the following antennas proc	duce a vertical radiation pattern?
a) Dipole antenna b) Yagi antenna	© Marconi antenna d) Hertz antenna
o) rugi untomu	
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	SRI BHARATHI ENGLIS
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	Kaikkurchi - 622 303, Pudukkottai Dt.



a)Field patterns

b)Power patterns

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Name of the Student: S. SARADHA Year/Sem: TV VIII AU Register Number: 912615106701 Value Added Course on "Antenna Design using HFSS" MCQ QUESTIONS (20X1 = 20 Marks) 1. EIRP in an isotropic antenna stands for (a) Effective isotropic radiated power c)Entropic isotropic radiated power b)Equivalent isotropic radiation power d)Equivalent isolated radiated power 2. What is the gain factor (in dB) of an isotropic radiator in all directions? a)1 c)Infinity b)0 (d))0db 3. What is the gain factor of an isotropic radiator in all directions? (a)1 c)Infinity b)0 d)0db 4. What is the shape of isotropic radiation when observed in 3D? (a)Doughnut shaped c)Figure of Eight b)Spherical d)Circle 5. Isotropic radiation is also known as (a)Omni-directional radiation c)Tri-directional radiation b)Bi-directional radiation d)None of the above 6. The characteristics of an antenna's radiation pattern can be represented in _____ ways. a)2 c)4 d)4 7. Transmitting antenna has which of the following parameter as a basic requirement. a)Side lobes are low c)High SNR value (b)Efficiency is high d)High SNR value 8. Which of the following is an equation for ERP of an isotropic antenna? (a) ERP(dBW) = EIRP(dBW) - 2.15dBic)ERP(dBW) = EIRP (dBW) + 2.15dBi b)ERP(dBW) = EIRP (dBW) -3.15dBi d)ERP(dBW) = EIRP (dBW) * 2.15dBi9.Radiation patterns can be represented in terms of

(c)Both a and b

d)Direction pattern

Dr. S.THILAGAVATHI M.E.,Ph.D.,
PRINCIPAL
SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkottai Dt.



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P				
10.A 2-D radiat	ion pattern gra	ph contains how ma	any coordinates?	
a)2	b)3	c)5	(1)	
M ntonno con	a ha nalanizad i			
	be polarized i			
a)3	(6)2	c)5	d)1	
12. An example	of circular pol	arization is		
(a)GPS			c)TV signals	
b)Radio way	/e		d)Mobile communication	signals
13. Which of th	e following is t	the frequency of ho	rizontal polarization?	
(a)1 GHz			c)15 GHz	
b)10 GHz			d)20 GHz	
0)10 0112			d)20 GHZ	
14. Magnetic fi	eld in EM wave	e is plotted on	axis.	
a) X-axis			c)Z-axis	
(b) Y-axis			d)Either a or b	
(b) 1-dxis			d)Either a or o	
15. Units of Po	vnting vector is	db0(b		
(a) W/m2	b)W/m	c)m/W	d)wm	
, 0		CHE THE DOVINGO THE	w bolloca vigorios la egs	
	length is bigger	than the length of	dipole then it is termed as a	type of
dipole.				
a)Infinitesin	nal dipole		c)Short dipole	
b)Long dipo	le		(d)Any of the above	
17. What is the	range of freque	ency in a V-shaped	antenna that operates?	
a)33KHz to		NA SIGNAL SHOPE IN	c) 30 MHz to 300 GHz	
(b)3 to 30 M			d)31KHz to 300 GHz	
(3)3 to 30 111	m hamacaic		u)311112 to 300 GHZ	
10 30/1 4 3 4	1	1.16 11.1		
	beam width to	r a half wave dipole		
@ 90°			c) 50°	
b) 180°			d) 250°	
19. What is the	impedance of	the folded dipole ar	tenna?	
a) 50Ω			© 300Ω	
b) 100Ω			d) 20Ω	
20 Which afth	na fallanina	tannaa nua daasa	outical radiation nattons?	T.W.BEFFREE CO.
	_	tennas produce a ve	ertical radiation pattern?	
a) Dipole a			© Marconi antenna	11~/
b) Yagi ant	enna		d) Hertz antenna	the t

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PRINCIPAL
SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkotiai Dt.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONENGINEERING ACADEMIC YEAR EVEN SEMESTER (2018-2019)

MARK SHEET FOR VALUE ADDED COURSE-ANTENNA DESIGN USING HIGH FREQUENCY

SIMULATION SOFTWARE

S.NO REGISTER NUMBER	NAME	NAME Q.	YEAR Attendance (A)		VAC -MC	OVERALL MARK(100)		
			No.of Sessions Attented	Marks (100)	No.of Correct Answer	Marks (100)	(50% of A + 50% of B)	
1	912617106001	ABIRAMI.S	II /ECE	10	100	16	80	90
2	912617106002	ABISHEKA.S	II /ECE	10	100	18	90	95
3	912617106003	ATSHAYA.R	II /ECE	8	80	17	85	83
4	912617106004	BAVADHARANI.A	II /ECE	10	100	14	60	80
5	912617106005	BHUVANESHWARI.B	II /ECE	8	80	13	65	73
6	912617106006	DHIVYA.L	II /ECE	9	90	15	75	83
7	912617106007	GOWSALYA.D	II /ECE	10	100	16	80	90
8	912617106009	INDHUMATHI.S	II /ECE	9	90	15	75	83
9	912617106010	KANIMOZHI.D	II /ECE	9	90	15	75	83
10	912617106011	KAVYA.C	II /ECE	10	100	19	95	98 /
11	912617106012	KEERTHANA.G	II /ECE	10	100	₽7 S.T	HIL883AV	ATHI MBE., Ph.
12	912617106013	MAHESHWARI.G	II /ECE	10	100		1 1 1 1 1 1 1 1	CIPAL ENGIN EÉRING

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13	912617106014	MANOHARI.M	II /ECE	10	100	14	70	85
14	912617106015	MARAGATHALAKSHMI.S	II /ECE	9	90	13	65	78
15	912617106017	SAFRIN NISHA.S	II /ECE	10	100	16	80	90
16	912617106018	SUBASHINI.M	II /ECE	10	100	13	65	83
17	912617106019	SUBASHINI.T	II /ECE	10	100	14	70	85
18	912617106020	VINTHIYA.R	II /ECE	10	100	19	95	98
19	912616106001	ABINAYA.R	III /ECE	10	100	18	90	95
20	912616106002	AGALYA.A	III /ECE	10	100	16	80	90
21	912616106003	ATCHAYA.G	III /ECE	10	100	14	60	80
22	912616106004	DEEPA.N	III /ECE	10	100	18	90	95
23	912616106005	DHARANIYA.A	III /ECE	10	100	14	70	85
24	912616106006	JEEVITHA.U	III /ECE	10	100	14	70	85
25	912616106007	MAHESWARI.V	III /ECE	8	80	15	75	78
26	912616106008	PAZHANIYAMMAL.R	III /ECE	10	100	18	90	95
27	912616106009	PRIYANKA.E	III /ECE	10	100	16	80	90
28	912616106010	ROJA.A	III /ECE	10	100	19	95	98
29	912616106011	SHANMUGAPRIYA.R	III /ECE	10	100	12	60	80
30	912616106012	SHIYAMALA.E	III /ECE	10	100	14	70	82
31	912616106013	SIVA BHARATHI.P	III /ECE	10	100	13	65	83
32	912616106014	SIVARUBINI.S	III /ECE	10	100	19	95	98
33	912616106015	THENMOZHI.A	III /ECE	10	100	13	65	83
34	912616106016	VINCY.A	III /ECE	10	100	14	70	85 S.TH

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ູ35	912616106302	SANKAVI M	III /ECE	10	100	14	70	85
36	912615106001	AARTHI .M	IV/ECE	9	90	17	75	83
37	912615106002	ABIRAMI .C	IV/ECE	10	100	18	90	95
38	912615106004	AKILA .S	IV/ECE	10	100	16	80	90
39	912615106005	ARTHI .M	IV/ECE	10	100	15	75	- 88
40	912615106006	BAVADHARANI .M	IV/ECE	10	100	14	70	85
41	912615106007	DIVYABHARATHI .S	IV/ECE	9	90	16	80	85
42	912615106008	JAGADESWARI .K	IV/ECE	10	100	15	75	88
43	912615106009	MEENAKSHI .R	IV/ECE	10	100	17	85	93
44	912615106010	MEENAL .T	IV/ECE	10	100	15	75	88
45	912615106012	SARGUNAVALLI.C	IV/ECE	10	100	13	65	83
46	912615106013	THENMOZHI .K	IV/ECE	8	80	14	70	75
47	912615106014	VENNILA .K	IV/ECE	10	100	18	90	95
48	912615106301	MANIMEGALAI .S	IV/ECE	9	90	15	75	83
49	912615106701	SARADHA .S	IV/ECE	10	100	18	90	95
50	912615106702	KAVIYA. S	IV/ECE	10	100	14	70	85

VAC Coordinator

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. HOD/ECE
HOD / ECE
SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
KAIKKURICHI,
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Criteria 2

Teaching-Learning and Evaluation

350

Key Indicator- 2.3. Teaching- Learning Process (40)

2018-2019

ELECTRONICS AND COMMUNICATION ENGINEERING PARTICIPATIVE LEARNING WORKSHOP



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ACADEMIC YEAR 2018-2019

S.No Register No		Student Name	Year/Sem	Name of the Learning Method		
1	912615106001	AARTHI .M				
2	912615106002	ABIRAMI .C	IV/VII	Workshop-Filter design using MATLAB		
3	912615106004	AKILA .S				
4	912615106005	ARTHI .M				
5	912615106007	DIVYABHARATHI .S				
6	912615106008	JAGADESWARI .K				
7	912615106010	MEENAL .T				
8	912615106702	KAVIYA. S				
9	912615106013	THENMOZHI .K				
10	912615106014	VENNILA .K				
11	912615106006	BAVADHARANI .M	IV/VII	W. I.I. I.T.		
12	912615106701	SARADHA .S				
13	912615106009	MEENAKSHI .R				
14	912615106301	MANIMEGALAI .S		Workshop-IoT using raspberry		
15	912615106012	SARGUNAVALLI .C				
16	912615106014	VENNILA .K				
17	912616106002	AGALYA.A		Workshop-IoT using raspberry I		
18	912616106007	MAHESWARI.V	III/V			
19	912616106014	SIVARUBINI.S				

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. HoD/ ECE HOD / ECE SRI BHARATHI ENGINEERI COLLEGE FOR WOMEN KAIKKURICHI. PUDUKKOTTAI - 622 303



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MATLAB" 1 eld on 25 th July 2018.

Mr.P.Sabarish Coordinator

Dr. A ajkumar

HOIVEEE Dr. S.THILAGAVATHIME., Ph.D.,

Dr.S.Muruge nandam

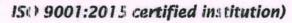
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Mr.P.Sabarish Coordinator

Dr. A. ajkumar Hbl VEEE

Dr.S.Muruge nandam
Dr. S.THILAGAVATHIM.E. Ph.D. Principal

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Nr.P.Sabarish Coordinator

A.Rakumar HoD.EEE Pr. S.THILAGAVATHIM.E.,Ph.D.

Dr.S.Murugamındam

Principal

PRINCIPAL SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.





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Mr.P.Sabarish Coordinator

HOLVEEE

Dr. S.THILAGAVATHI M.E., Ph.D.,

Dr.S.Muruga nandam

Principal

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



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Nr.P.Sabarish Coordinator

Dr A.R. jkumar

Dr. S.THILAGAVATHIME. Ph.D. P

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kalkkurchi - 622 303, Pudukkottai Dt. r.S.Muruga nandam

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Mr.P.Sabarish Coordinator

n. A jajkumar Hbl VEEE

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

Dr.S.Murug: nandam





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Mr.P.Sabarish Coordinator A jajkumar Hbl VEEE

Dr.S.Muruga nandam
Principal

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SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkoitai Dt.



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Mr.P.Sabarish Coordinator

. A ajkumar

HOLVEEE Dr. S.THILAGAVATHI M.E., Ph.D.,

M.E., Ph.D., Principal

Dr.S.Muruga nandam

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workshop on "Filter design and THD analysis for AC-EC converter using
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Mr.P.Sabarish Coordinator

Dr. A ajkumar

HOIVEEE Dr. S.THILAGAVATHI M.E. P

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Puddakoka Dt. Dr.S.Muruga nandam Principal



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workshop on "Filter design and THD analysis for AC-DC converter using
MATLAB" held on 26 th July 2018.

Mr.P.Sabarish Coordinator Dr. A.Rajkumar HoD/EEE

Dr.S.Muruganandam Principal

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING

Kaikkurehi - 622 303, Pudukkottai Di





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Lena Vilakku, Pilivalam PO., Thirumayam Tk., Pudukkottai, Tamil Nadu, India. Pin - 622 507.

Phone: 04333 - 294400. e-mail: info@mzcet.in,

website: www.mzcet.in, Fax: +91 8030723678.



This is to certify that BAVADHARANI. M - IV YEAR | ECE of SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN has participated in the one day workshop on IoT using Raspberry Pi organised by the Department of Computer Science and Engineering in association with the Computer Society of India at Mount Zion College of Engineering and Technology, on August 29, 2018.

A-MP/29/8/18 COORDINATOR

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.





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Phone: 04333 - 294400. e-mail: info@mzcet.in,
website: www.mzcet.in, Fax: +91 8030723678.



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participated in the one day workshop on IoT using Raspberry Pi organised by the Department of

Computer Science and Engineering in association with the Computer Society of India at

Mount Zion College of Engineering and Technology, on August 29, 2018.

A: HH29/8/19 COORDINATOR

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kalkkurchi - 622 303, Pudukkottai Dt.





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Lena Vilakku, Pilivalam PO., Thirumayam Tk., Pudukkottai, Tamil Nadu, India. Pin - 622 507.

Phone: 04333 - 294400. e-mail; info@mzcet.in,

website: www.mzcet.in, Fax: +91 8030723678.



This is to certify that MEENAKSHI.R	IV YEAR / ECE of
- SRI BHARATHI ENGINEERING COLLEGE FOR	has has
participated in the one day workshop on loT using Raspber	ry Pi organised by the Department of
Computer Science and Engineering in association with	the Computer Society of India at
Mount Zion College of Engineering and Technology, on Aug	ust 29, 2018.

COORDINATOR

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukköttai Dt.





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Lena Vilakku, Pilivalam PO., Thirumayam Tk., Pudukkottai, Tamil Nadu, India. Pin - 622 507.

Phone: 04333 - 294400. e-mail: info@mzcet.in,

website: www.mzcet.in, Fax: +91 8030723678.



This is to certify that	NIMEGALALS	YEAR EC	E	of
SRIBHARATH! ENGINEERI	NG COLLEGE	FOR WO	MEN	has
participated in the one day workshop on IoT	using Raspberry P	i organised b	y the Depart	ment of
Computer Science and Engineering in as	sociation with the	Computer	Society of	India at
Mount Zion College of Engineering and Tech	nnology, on August	29, 2018.		

A-HP/29/8/19 COORDINATOR

Dr. S.THILAGAVATHI M.E., Ph.D.,

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. PRINCIPAL \





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Phone: 04333 - 294400. e-mail: info@mzcet.in,

website: www.mzcet.in, Fax: +91 8030723678



This is to certify that SARGUNAVALLI.C. SER FOR WOMEN has SRIBHARATHI ENGINEERING COLLEGE FOR WOMEN has participated in the one day workshop on IoT using Raspberry Pi organised by the Department of Computer Science and Engineering in association with the Computer Society of India at Mount Zion College of Engineering and Technology, on August 29, 2018.

A-MM29/8/19 COORDINATOR

Dr. S.THILAGAVATHI M. ... Ph.D.

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. PRINCIPAL \





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Lena Vilakku, Pilivalam PO., Thirumayam Tk., Pudukkottai, Tamil Nadu, India. Pin - 622 507.

Phone: 04333 - 294400. e-mail: info@mzcet.in, website: www.mzcet.in, Fax: +91 8030723678.



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SRIBHARATHI ENGINEERI	NG COLLEGE	FOR W	OMEN	has
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A-MM29/8/19 COORDINATOR

Dr. S.THILAGAVATHI M.E., Ph.D.,

PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

Kaikkurchi - 622 303, Pudukkottai Dt.





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Lena Vilakku, Pilivalam PO., Thirumayam Tk., Pudukkottai, Tamil Nadu, India. Pin - 622 507.

Phone: 04333 - 294400. e-mail: info@mzcet.in,

Phone: 04333 - 294400. e-mail: info@mzcet.in, website: www.mzcet.in, Fax: +91 8030723678.



This is to certify that __AGALYA A - TIT_ YEAR | ECE _______ of _______ GRI_BHARATHI ENGINEERING COLLEGE FOR WOMEN ______ has participated in the one day workshop on IoT using Raspberry Pi organised by the Department of Computer Science and Engineering in association with the Computer Society of India at Mount Zion College of Engineering and Technology, on August 29, 2018.

A. Hel29/8/19 COORDINATOR

Dr. S.THILAGAVATHI M.E., Sh.D.,
PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kalkkurchi - 622 303, Pudukkottai Dt.





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This is to certify that MAHESWARI.Y - III YEAR ELE	of				
SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN h	as				
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COORDINATOR

Dr. S.THILAGAVATHI M.E., Ph.D.,

PRINCIPAL

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Lena Vilakku, Pilivalam PO., Thirumayam Tk., Pudukkottai, Tamil Nadu, India. Pin - 622 507.

Phone: 04333 - 294400. e-mail: info@mzcet.in,

website: www.mzcet.in, Fax: +91 8030723678.



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A-LAPOR 18 19 COORDINATOR

Dr. S.THILAGAVATHIME., Ph.D.

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt. PRINCIPAL \