

SRI BHARATHI

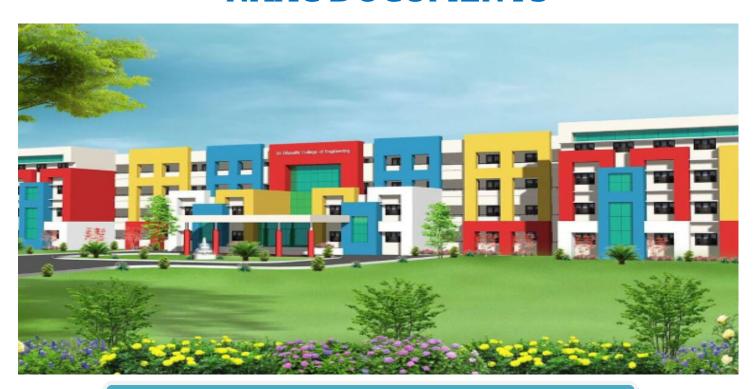
ENGINEERING COLLEGE FOR WOMEN

(Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai)

Kaikkurichi, Pudukkottai -622 303

www.sbec.edu.in

NAAC DOCUMENTS



Quality Indicator Frame Work

Criterion – 1 CURRICULAR ASPECTS

Submitted by

IQAC
Internal Quality Assurance Cell

Sri Bharathi Engineering College for Women



SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) KAIKKURUCHI, PUDUKOTTAI – 622 303

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019 / ODD SEMESTER

1.2 Academic Flexibility (30)

1.2.1 Number of Certificate/Value added courses offered and online courses of MOOCs, SWAYAM, NPTEL etc. (where the students of the institution have enrolled and successfully completed during the last five years)

AND

1.2.2 Percentage of students enrolled in Certificate/ Value added courses and also completed online courses of MOOCs, SWAYAM, NPTEL etc. as against the total number of students during the last five years

VAC Title:	DIG	DIGITAL SYSTEM DESIGN WITH XILINX									
Resource Per	rson:	Er.A.GANESAN, Software Engineer, Maria Academy,Chennai.									
Date of cond	uct fro	m :	18.06.201	18	To:	22.06	.2018	Duration:	30 Hours		
Organized D	epartn	nent :	ELECTI	RONICS AN	D COM	IMUN	ICATION E	NGINEERI	NG		
Participant Y	Participant Year: 2/3/4		Semester:	ODD		No. of Students Registered : 50					
Venue: Se	Seminar Hall, ,Ground Floor, SBECW										

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

DEPARTMENT CIRCULAR

Date:08.06.2018

Value Added Course offered by the Department of ECE will be conducted for all Second, Third and Final year students on "Digital System Design with Xilinx" in association with Maria Academy from 18.06.2018 to 22.06.2018. Certificates will be issued to the eligible participants at the end of the course.

S.No	Name of the Course	Resource Person
1	Digital System Design with Xilinx	Er.A.GANESAN, Software Engineer, Maria Academy, No 58, 17, S Usman Road, Near Bus stand, Kannammapet, T. Nagar, Chennai 600059. Tamil Nadu . Mail.Id: mariatrainingacademy@gmail.com

Cc:

Principal's Office

IQAC Coordinator

II ,III & IV Year ECE Students

Notice Board

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI.

PUDUKKOTTAI - 622 303.

Class In charges- II ,III &IV Year Dr. S.THILAGAVATHTM.E. Ph.D., PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu - 622 303, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING **ACADEMIC YEAR 2018-2019/ODD SEMESTER**

Value Added Course on "Digital System Design With Xilinx"

SYLLABUS

S.NO	TOPIC COVERED	DURATION (in hours)	DATE
1	Evolution and Basics of ICs and Digital System Design, Evolution of Integrated Circuits ,Digital Logic Family	2	18.06.2018
2	Basics of Logic gates – Boolean Algebra – Digital circuit design using Boolean Algebra and K – Map.	1	18.06.2018
3	ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques.	3	18.06.2018
4	Architecture of ROM – ROM Programming – Architecture of SPLDs – SPLDs programming	3	19.06.2018
5	Architecture of CPLDs – Basics of FPGAs– Structure of FPGAs	3	19.06.2018
6	Verilog Coding and Simulation of Digital Systems using Xilinx	3	20.06.2018
7	Verilog HDL Basics- Gate level, Data flow and Behaviour Modelling – Simulation of simple digital circuits	3	20.06.2018
8	Implementation of Digital circuits in FPGA processor Spartan 6 FPGA features	3	21.06.2018
9	Education FPGA kit – FPGA pin assignment	3	21.06.2018
10	Implementation of simple digital circuits using FPGA hardware	3	22.06.2018
11	Interfacing Input /Output devices with FPGA	3	22.06.2018
	Total Hours		30

oordinator

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL

SRI BHARATHI ENGINEERING **COLLEGE FOR WOMEN** Kaikkurchi - 622 303, Pudukkottai Dt.

LEGE FOR WOMEN KAIKKURICHI HOUKKOTTAL-672 333



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DEPARTMENT OF ELECTRONICS AN COMMUNICATIONENGINEERING ACADEMIC YEAR ODD SEMESTER (2018-2019)

STUDENT PARTICIPATION LIST FOR VALUE ADDED PROGRAM

Digital System Design With Xilinx

S.NO	REG.NO	NAME	YEAR & BRANCH		
13036	912617106001	ABIRAMI.S	II&ECE		
2	912617106002	ABISHEKA.S	II&ECE		
3	912617106003	ATSHAYA.R	II&ECE		
4	912617106004	BAVADHARANI.A	II&ECE		
5	912617106005	BHUVANESHWARI.B	II&ECE		
6	912617106006	DHIVYA.L	II&ECE		
7	912617106007	GOWSALYA.D	II&ECE		
8	912617106009	INDHUMATHI.S	II&ECE		
9	912617106010	KANIMOZHI.D	II&ECE		
10	912617106011	KAVYA.C	II&ECE		
11	912617106012	KEERTHANA.G	II&ECE		
12	912617106013	MAHESHWARI.G	II&ECE		
13	912617106014	MANOHARI.M	II&ECE		
14	912617106015	MARAGATHALAKSHMI.S	II&ECE		
15	912617106017	SAFRIN NISHA.S	II&ECE		
16	912617106018	SUBASHINI.M	II&ECE		
17	912617106019	SUBASHINI.T	II&ECE		
18	912617106020	VINTHIYA.R	II&ECE		
19	912616106001	ABINAYA.R	III&ECE		
20	912616106002	AGALYA.A	III&ECE		
21	912616106003	ATCHAYA.G	III&ECE		
22	912616106004	DEEPA.N	III&ECE		
23	912616106005	DHARANIYA.A	III&ECE		
24	912616106006	JEEVITHA.U	III&ECE		
25	912616106007	MAHESWARI & THILAGA	VATHI & HCPh.		

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi- 622 303, Pudukkottai Dt.

S.NO	REG.NO	NAME	YEAR & BRANCH		
26	912616106008	PAZHANIYAMMAL.R	III &ECE		
27	912616106009	PRIYANKA.E	III &ECE		
28	912616106010	ROJA.A	III &ECE		
29	912616106011	SHANMUGAPRIYA.R	III &ECE		
30	912616106012	SHIYAMALA.E	III&ECE		
31	912616106013	SIVA BHARATHI.P	III&ECE		
32	912616106014	SIVARUBINI.S	III&ECE		
33	912616106015	THENMOZHI.A	III&ECE		
34	912616106016	VINCY.A	III&ECE		
35	912616106302	SANKAVI M	III&ECE		
36	912615106001	AARTHI .M	IV&ECE		
37	912615106002	ABIRAMI .C	IV&ECE		
38	912615106004	AKILA .S	IV&ECE		
39	912615106005	ARTHI .M	IV&ECE		
40	912615106006	BAVADHARANI .M	IV&ECE		
41	912615106007	DIVYABHARATHI .S	IV&ECE		
42	912615106008	JAGADESWARI .K	IV&ECE		
43	912615106009	MEENAKSHI .R	IV&ECE		
44	912615106010	MEENAL.T	IV&ECE		
45	912615106012	SARGUNAVALLI.C	IV&ECE		
46	912615106013	THENMOZHI .K	IV&ECE		
47	912615106014	VENNILA .K	IV&ECE		
48	912615106301	MANIMEGALAI .S	IV&ECE		
49	912615106701	SARADHA .S	IV&ECE		
50	912615106702	KAVIYA. S	IV&ECE		

VAC Coordinator

HoD/ECE

HOD / ECE

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI, PUDUKKOTTAI - 622 303

Dr. S.THILAGAVATHI M.E., Ph.D.,

PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING ACADEMIC YEAR ODD SEMESTER (2018-2019)

ATTENDANCE SHEET FOR VALUE ADDED COURSE -DIGITAL SYSTEM DESIGN WITH XILINX

S.No	REG. NO	NAME	YEAR/	18.6	.2018	19.6	.2018	20.6	2018	21.6.	2018	22.6	5.2018	NO. OF	SIGN OF
4	arse1e16e00e	TERAILIIVO	BRANCH	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	F.N	A.N	- SESSIONS ATTENDED	STUDENT
1	912617106001	ABIRAMI.S	II /ECE	1	1	1	1	1	1	1	1	,	/	10	S. Abiram
2	912617106002	ABISHEKA.S	II /ECE	1	1	1	1	1	1	1	1	/	,	10	S. Pho
3	912617106003	ATSHAYA.R	II /ECE	a	1	,	1	,	,	,	1	1	,	9	R. Atchy
4	912617106004	BAVADHARANI.A	II /ECE	a	1	1	1	1	1	1	,	,	,	9	6. Baralle
5	912617106005	BHUVANESHWARI.B	II /ECE	1	1	,	,	1	/	1	1	1	1	10	B'Bhuranes
6	912617106006	DHIVYA.L	II /ECE	1	,	1	,	1	1	1	,	1	,	10	1 Divar
7	912617106007	GOWSALYA.D	II /ECE	1	1	,	,	7	,	,	,	1	1	10	D. Curisal
8	912617106009	INDHUMATHI.S	II /ECE	1	1	1	1	a	,	,	,	,	,	9	S. Indlumi
9	912617106010	KANIMOZHI.D	II /ECE	/	1	1	1	1	7	,	1	1	,	i i	D. Kanno
10	912617106011	KAVYA.C	II /ECE	1	/	,	1	1	1	,	,	1	1		C. Karyo
11,	912617106012	KEERTHAN & GS. THIL	1 3 mg 1 2 1 2 1 mg 1 mg 1 mg 1 mg 1 mg 1 m			,	1	1	,	,	,	1	1	10	G. Koerthour
12	912617106013	MAHESHWARI. GRIBHA	RATH/BENEGIN EGE FOR WO 1-622303, Pudu			,	,	1	1	1	,	,	1		G. Maliosco

	TELEVILLE INVESTOR NA	A THE PERSON OF		CONTRACTOR OF							1		T		
13	912617106014	MANOHARI.M	II /ECE	1	1	1	1	1	1	1	1	1	1	10	M. Nemonia
14	912617106015	MARAGATHA LAKSHMI.S	II /ECE	a	a	1	1	1	1	1	1	1	1	8	S. Masageth
15	912617106017	SAFRIN NISHA.S	II /ECE	1	1	1	1	1	,	1	1	1	1	10	S. Safan Di
16	912617106018	SUBASHINI.M	II /ECE	1	1	1	1	1	1	1	1	1	1	10	M. Subashi
17	912617106019	SUBASHINI.T	II /ECE	1	1	,	1	a	a	1	1	,	1	8	T. Subi
18	912617106020	VINTHIYA.R	II /ECE	1	1	1	,	1	,	1	,	1	1	10	Revinter
19	912616106001	ABINAYA.R	III/ECE	1	1	,	1	1	1	,	1	1	1	10	R. Abacy
20	912616106002	AGALYA.A	III/ECE	a	a	,	1	1	1	1	1	1	1	8	A. angalya
21	912616106003	ATCHAYA.G	III/ECE	1	/	1	1	1	1	1	1	1	1	10	6. Helas
22	912616106004	DEEPA.N	III/ECE	1	1	,	1	1	1	1	1	1	1	10	X. Daga
23	912616106005	DHARANIYA.A	III/ECE	1	1	1	1	a	,	1	1	1	1	9	A. Dharan
24	912616106006	JEEVITHA.U	III/ECE	1	,	1	1	1	1	1	1	1	1	10	U. Feesith
25	912616106007	MAHESWARI.V	III/ECE	1	1	1	1	a	a	1	1	1	,	8	V. Maheur
26	912616106008	PAZHANIYAMMAL.R	III/ECE	,	1	1	1	1	1	1	1	1	/	10	Paghout
27	912616106009	PRIYANKA.E	III/ECE	1	,	1	,	1	1	1	1	1	1	10	Poryant
28	912616106010	ROJA.A	III/ECE	1	1	1	1	1	1	1	1	1	/	10	Rote
29	912616106011	SHANMUGAPRIYA.R	III/ECE	1	,	,	1	1	1.	1	1	1	1	10	Shawkiy
30	912616106012	SHIYAMALA.E	III/ECE	1	,	1	1	1	1	.1	1	1	1	10	E. Quent
31	912616106013	SIVA BHARATHI.P	III/ECE	1	1	1	1	1	1	1	,	1	1	10	P.Sahlu
32	912616106014	SIVARUBINI.S	III/ECE	1	,	1	1	1	1	1	1	,	1	10	SILA
33	912616106015	THENMOZHI.A S	LEHARATHI	ENGINI OR WO	EERING	a	a	/	1	1	1	1	1	8	7/2

Kailkurchi - 622 303, Pudukkottai Dt.

34	912616106016	VINCY.A	III/ECE	1	,	,	1	,	,	1	1	,	,	ľo	Vency &.
35	912616106302	SANKAVI M	III/ECE	1	1	7	1	,	1	1	,	1	1	lo	M. Santan
36	912615106001	AARTHI .M	IV/ECE	a	1	1	1	1	,	1	,	1	,	9	H. Garthi
37	912615106002	ABIRAMI .C	IV/ECE	1	1	,	,	1	,	1	,	,	,	In	Abisanie
38	912615106004	AKILA .S	IV/ECE	1	1	,	,	,	1	1	,	. /	,	10	Akila . S
39	912615106005	ARTHI .M	IV/ECE	,	1	./	,	1	,	1		1	1	10	Aothi.M
40	912615106006	BAVADHARANI .M	IV/ECE	1	1	1	1	1	,	1	1.	1	,	10	Ben Dan
41	912615106007	DIVYABHARATHI .S	IV/ECE	1	1	1	,	1	,	. /	,	1	,	10	S. Day of
42	912615106008	JAGADESWARI .K	IV/ECE	1	1	1	/	1	,	1	,	1	,	10	Fagadehin
43	912615106009	MEENAKSHI .R	IV/ECE	,	1	,	,	1	,	a	a	1	,	2	Nechalin
44	912615106010	MEENAL .T	IV/ECE	1	1	,	/	1	,	1	,	1	,	10	T. Mand
45	912615106012	SARGUNAVALLI.C	IV/ECE	a	æ	,	1	/	,	1	,	1	1	8	C. Stroge De
46	912615106013	THENMOZHI.K	IV/ECE	1	1	1	,	1	,	1	,	1	ß	10	K. The
47	912615106014	VENNILA .K	IV/ECE	1	1	,	,	/	,	1	,	,	,	10	Valinila.
48	912615106301	MANIMEGALAI .S	IV/ECE	,	/	,	,	1	,	a	,	1	,	9	Her
49	912615106701	SARADHA .S	IV/ECE	1	1	,	/	/	,	1	,	,	,	10	Carothan
50	912615106702	KAVIYA. S	IV/ECE	1	1	1	1	/	1	,	1	/	1	10	Skange

SRI BHARATHI ENGINEERING
COLLEGE FOR WOMEN
Kaikkurchi - 622 303, Pudukkottai Dt.

VAC Coordinator

HoD/ ECE HOD / ECE SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN KAIKKURICHI.

(Approved by AICTE, New Delhi, Affiliated to Anna University, Chennai-25) Kaikkurichi, Pudukkottai, Tamil Nadu - 622 303, India

Report on Value Added Course

Title:

Digital System Design with Xilinx

Resource Person:

Mr.A.GANESAN Software Engineer. Maria Academy,

T. Nagar, Chennai 600059.

Date of conduct from:

18.06.2018

To: 22.06.2018 Duration:

30 Hours

Organized Department:

Electronics and Communication Engineering

Participant Year:

2/3/4

Semester:

ODD

No. of Students Registered:

50

Venue:

Seminar Hall, Ground Floor, SBECW

Outcome of Value Added Course (VAC): At the end of Course , Students can able to

- Design the system meeting the specifications
- Design the data path and the controller(s) to implement the functionality.
- Develop Verilog based programs and simulate digital circuits.
- Analyze a VHDL code and infer what circuit a synthesis tool might generate out of a code.
- Implement digital circuits in Xilinx FPGA processor using Hardware description Language experimentally.
- Design and code to exploit the architectural features of FPGA.

No. of students successfully completed the VAC course is 50 Students based on the following Assessment process.

Assessment Process

- Students securing more than 60% on total score and secured more than 75% in attendance is eligible to receive the certificate for the VAC course conducted
- Total Score = (0.5 *Attendance in VAC out of 100 percentage + 0.5 *Test mark in VAC out of 100 marks)

ordinator

HOD / ECE SRI BHARATHI ENGINEERING

COLLEGE FOR WOMEN

PUDUKKOTTAI - 622 308

KAIKKURICHI,

Dr. S.THILAGAVATHI M.E., Ph.D. PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

Kaikkurchi - 622 303, Pudukkottai Dt.



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ATCHAYA.G, III YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

> Dr. S.THILAGAVATHI M.E., Ph.D., PRINCIPAL SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN

Kaikkurchi - 622 303, Pudukkottai Dt.

RESOURCE PERSON

T. NAGAR, CHENNAI 600059. TAMIL NADU. MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. ABIRAMI.S, II YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph.D.)
PRINCIPAL

SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

Ganesan RESOURCE PERSON



CERTIFICATE OF PARTICIPATION

This is to Certify that Mr/Ms. VENNILA .K, IV YEAR ECE, from Sri Bharathi Engineering College for Women, has successfully completed 5 days Value Added Course on Digital System Design With Xilinx Conducted from 18.06.2018 to 22.06.2018 during the academic year 2018-2019.

Dr. S.THILAGAVATHI M.E., Ph.D.,
PRINCIPAL
SRI BHARATHI ENGINEERING

COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

T. NAGAR, CHENNAI 600059. TAMIL NADU.

MAIL. ID: MARIATRAININGACADEMY@GMAIL.COM

Ganesan RESOURCE PERSON



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Nam	e of the Student:	Year/Sem:
AU F	Register Number:	
	Value Added Course on "l	Digital System Design with Xilinx"
	MCQ QUESTI	ONS (25X1 = 25 Marks)
1.	Which of the following options come Electronics?	es under the non – saturated logic family in Digital
	a) Emitter – coupled Logicb) High-Threshold Logic	c) Integrated – injection Logicd) Diode – Transistor Logic
2.	Which characteristic of IC in Digita particular transistor?	l Circuits represents a function of the switching time of a
	a) Fan – out	c) Power dissipation
	b) Fan – in	d) Propagation delay
3.	Which gates in Digital Circuits are reflop?	equired to convert a NOR-based SR latch to an SR flip-
	a) Two 2 input AND gates	c) Two 2 input OR gates
	b) Two 3 input AND gates	d) Two 3 input OR gates
4.	What must be used along with synch	ronous control inputs to trigger a change in the flip flop?
	a) 0	c) Clock
	b) 1	d) Previous output
5.	What are the basic gates in MOS log	ic family?
	a) NAND and NOR	c) NAND and OR
	b) AND and OR	d) AND and NOR
6.	Which of the following is only prede	fined physical literal in VHDL?
	a) Voltage	c) Current
	b) Time	d) Distance
7.	Access types are similar to	_ in traditional programming languages.
	a) Pointers	c) Structures
	b) Arrays	d) Files
8.	Which of the following is default del	ay in VHDL?
	a) Inertial delay	c) Delta delay
	b) Transport delay	d) Wire delay
9.	Transport delay is a kind of	Mondamie (a.
	a) Synthesis delay	c) Inertial delay
	b) Simulation delayor S.THILAG	WATHIME PH Wire delay

PRINCIPAL
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10. A buff	er with single input A and single output B l	nas a delay of 20 nanosecond. If the value of
	A changes after 10 ns from 0 to 1 and it cha	
	he value of output B will be 1, if the transpo	
a) 20 n		c) 40 ns
b) 30 r	is 2 alive noised moteve langual.	d) Output will remain zero
11. The pr	ocess used for implementation of sequentia	I logic in VHDL is called process.
	uential process	c) Clocked process
b) Con	nbinational process	d) Unlocked process
12. A user	r doesn't want to use the IF statement for de	etecting clock edge. It is possible to do the
	y using any other keyword in VHDL.	orace program i-pagetti
a) True		b) False
10 01 1	we will to houselik a amoronyot amono tah	
13. PLA co		tro = ag 1 (s
	O and OR arrays	c) NOT and AND arrays
b) NAI	ND and OR arrays	d) NOR and OR arrays
14. A PLA	is similar to a ROM in concept except that	
	isn't capability to read only	c) It doesn't provide full decoding to the
variabl		Politing to Price Study in Lie Own City
b) It ha	asn't capability to read or write operation	d) It hasn't capability to write only
	ichionods control imputs to trigger a change	
15. The co	mplex programmable logic device contains	several PLD blocks and
a) A la	nguage compiler	c) Global interconnection matrix
b) ANI	D/OR arrays	d) Field-programmable switches
16. Which	type of device FPGA are?	
a) SLD	The state of the s	c) EPROM
b) SRC	DM	d) PLD
	sacinite physical intent is created and in visit to the	
	A, vertical and horizontal directions are sep	Control of the Contro
a) A lii		c) A strobe
b) A cl	nannel	d) A flip-flop
18. In a di	gital clock application, the basic frequency	must be divided down as
a) 1 Hz		c) 100 Hz
b) 60 F	Hz	d) 1000 Hz
10 11/1:1	votsbaste@ (o	valsk famon fan s
	among the following is a process of transform a set of logic equations?	orining design entry information of the
	ulation	c) Synthesis
	imization	d) Verification S THIL AGAVATHI M.E., Ph.D.
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s predominantly associated with c) CPLDs
d) All of the above
th the determination of resistance & capacitance of
c) Testing
d) Extraction
that gives the description of logic cells & their
c) Checklist
d) Dualist
is/are executed in physical design or layout synthesis zed circuit in target chip chip
esponsible for converting an un optimized boolean
c) Optimization
d) All of the above
aretools.
c) Both a and b
d) None of the above

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ACADEMIC YEAR 2018-2019/ODD SEMESTER

Value Added Course on "Digital System Design with Xilinx"

MCQ ANSWER KEY

1	A	6	В	11	С	16	D	21	D
2	D	7	A	12	A	17	В	22	A
3	A	8	A	13	A	18	A	23	С
4	С	9	D	14	C	19	С	24	A
5	A	10	В	15	С	20	В	25	В

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Name of the Student: C. Kavya Year/Sem: D/ TII

AU Register Number: 912617106011

Value Added Course on "Digital	al System Design with Xilinx"
MCQ QUESTIONS	(25X1 = 25 Marks)
Which of the following options comes under	er the non – saturated logic family in Digital
Electronics?	
(a) Emitter – coupled Logic	c) Integrated – injection Logic
b) High-Threshold Logic	d) Diode – Transistor Logic
2. Which characteristic of IC in Digital Circu particular transistor?	its represents a function of the switching time of a
a) Fan – out	c) Power dissipation
b) Fan – in	d) Propagation delay
3. Which gates in Digital Circuits are required flop?	to convert a NOR-based SR latch to an SR flip-
a) Two 2 input AND gates	c) Two 2 input OR gates
b) Two 3 input AND gates	d) Two 3 input OR gates
4 What must be used along with synchronous	control inputs to trigger a change in the flip flop?
a) 0	C) Clock
b) 1 lam shoold CLIT lessons anialana so	d) Previous output
, (G) Global suterconnection matrix	roughous sampled A (a
5. What are the basic gates in MOS logic fami	ly?
(a) NAND and NOR	c) NAND and OR
b) AND and OR	d) AND and NOR
6 Which of the following is only predefined p	hygical literal in VIIDI 2
a) Voltage	c) Current
(b) Time vel beingege ette engl	d) Distance
odorda-A (o	d) Distance
7. Access types are similar to in tra	ditional programming languages.
(a) Pointers	c) Structures
b) Arrays	d) Files
8. Which of the following is default delay in V	HDI 2
(a) Inertial delay	c) Delta delay
b) Transport delay	d) Wire delay
ss of transforming design alary hater matteriol the	
9. Transport delay is a kind of	administration in the second
a) Synthesis delay	c) Inertial delayDr. S.THILAGAVATHI M.E.,Ph.L.
B Simulation delay	d) Wire delay PRINCIPAL SRI BHARATHI ENGINEERING

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10. A buffer with single input A and single output B l	nas a delay of 20 nanosecond. If the value of
input A changes after 10 ns from 0 to 1 and it chan	nges again from 1 to 0 at 20 ns. At what
time, the value of output B will be 1, if the transpo	ort delay model is used?
a) 20 ns	c) 40 ns
(b) 30 ns	d) Output will remain zero
O a series of the series of th	a) Gutput Will Telliam 2010
11. The process used for implementation of sequentia	l logic in VHDL is called process.
a) Sequential process	© Clocked process
b) Combinational process	d) Unlocked process
A sign I would be be the best of the control of the	(A) Emitter - ecopted Logic
12. A user doesn't want to use the IF statement for de	etecting clock edge. It is possible to do the
same by using any other keyword in VHDL.	O
a) True	(b) False
12 81 4	
13. PLA contains	na Fan - out
(a) AND and OR arrays	c) NOT and AND arrays
b) NAND and OR arrays	d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except that	Call "Which gates in Digital Circuits at
a) It hasn't capability to read only	(c) It doesn't provide full decoding to the
variables	C) it doesn't provide full decoding to the
b) It hasn't capability to read or write operation	d) It hasn't capability to write only
b) it hash t capability to read of write operation	d) it hash t capability to write only
acts offices collects applies to reguer a catalge in the time to	
15. The complex programmable logic device contains	several PLD blocks and
a) A language compiler	© Global interconnection matrix
b) AND/OR arrays	d) Field-programmable switches
SO Fou CIVAVA	
16. Which type of device FPGA are?	
a) SLD	c) EPROM
b) SROM	d PLD
ACTIVATION OF THE PROPERTY OF	osatlo V (all
VI. In FPGA, vertical and horizontal directions are se	parated by
a) A line	c) A strobe
(b) A channel	d) A flip-flop
and the state of t	
18. In a digital clock application, the basic frequency	must be divided down as
a) 1 Hz	c) 100 Hz
b) 60 Hz	d) 1000 Hz
adapanimidhi .	
19. Which among the following is a process of transfer	orming design entry information of the
circuit into a set of logic equations?	Olginal seed weight in a page of
a) Simulation b) Optimization	(c) Synthesis
b) Optimization Dr. S.THILAGAZATH	d) Verification M.E., Ph.D.,
PRINCIPAL PRINCIPAL	
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Name of the Student: A Dharaniy	Year/Sem: 10/I
Name of the Student: A Dharan'y AU Register Number: 912616106	3005
Value Added Course on "Digital	
MCQ QUESTIONS (25X1 = 25 Marks)
1. Which of the following options comes under Electronics?	the non – saturated logic family in Digital
(a) Emitter – coupled Logic	c) Integrated – injection Logic
b) High-Threshold Logic	d) Diode – Transistor Logic
particular transistor?	s represents a function of the switching time of a
a) Fan – out	c) Power dissipation
(b) Fan – in	Propagation delay
3. Which gates in Digital Circuits are required t flop?	o convert a NOR-based SR latch to an SR flip-
(a) Two 2 input AND gates	c) Two 2 input OR gates
b) Two 3 input AND gates	d) Two 3 input OR gates
4 What must be used along with synchronous of	control inputs to trigger a change in the flip flop?
a) 0	© Clock
ice contains several PLD plocks and1 (d	d) Previous output
5. What are the basic gates in MOS logic family	b) AND/OR scrays
5. What are the basic gates in MOS logic familya) NAND and NOR	c) NAND and OR
(b) AND and OR	d) AND and NOR
a Parkom	
6. Which of the following is only predefined ph	ysical literal in VHDL?
a) Voltage	c) Current
(b) Time	d) Distance
7. Access types are similar to in trad	litional programming languages.
(a) Pointers	c) Structures
b) Arrays	d) Files
8. Which of the following is default delay in VI	IDL?
a) Inertial delay	c) Delta delay
(b) Transport delay	d) Wire delay
9. Transport delay is a kind of	sionalumie (p.
a) Synthesis delay	c) Inertial delay Dr. S.THILAGAVATHI M.E., Ph.I.
b) Simulation delay	d) Wire delay

(d) Wire delay

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10. A buffer with single input A and single output B has input A changes after 10 ns from 0 to 1 and it changes after 10 ns from 0 to 1	nges again from 1 to 0 at 20 ns. At what
time, the value of output B will be 1, if the transpo	
a) 20 ns	c) 40 ns
(b) 30 ns	d) Output will remain zero
11. The process used for implementation of sequentia	Llogio in VIIDI, is called
a) Sequential process	
b) Combinational process	© Clocked process d) Unlocked process
o) Comomational process	d) Officered process
12. A user doesn't want to use the IF statement for de same by using any other keyword in VHDL.	etecting clock edge. It is possible to do the
(a) True	b) False
<u></u>	A particular translator?
X13. PLA contains	no – na l (a
a) AND and OR arrays	c) NOT and AND arrays
b) NAND and OR arrays	d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except that	
a) It hasn't capability to read only	(c) It doesn't provide full decoding to the
variables	e) it doesn't provide fair decoding to the
b) It hasn't capability to read or write operation	d) It hasn't capability to write only
15. The complex programmable logic device containsa) A language compilerb) AND/OR arrays	© Global interconnection matrix d) Field-programmable switches
16 Which the of day in EDCA - 9	
16. Which type of device FPGA are?	A) EDDOM
a) SLD (b) SROM	c) EPROM
U) SKOW	d) PLD
17. In FPGA, vertical and horizontal directions are se	parated by
a) A line	c) A strobe
(b) A channel	d) A flip-flop
18. In a digital clock application, the basic frequency	must be divided down as
(a) 1 Hz	c) 100 Hz
b) 60 Hz	d) 1000 Hz
Gelay in VHDLY	valetalejen (a) Inerchischen von varietalejen (a)
19. Which among the following is a process of transfocircuit into a set of logic equations?	orming design entry information of the
a) Simulation	© Synthesis
b) Optimization	d) VerificationS.THILAGAVATHIME.,Pin.
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20. An Antifuse programming technology is predo	ominantly associated with
a) SPLDs	c) CPLDs
(b) FPGAs	d) All of the above
21. In VLSI design, which process deals with the	determination of resistance & capacitance of
interconnections?	
a) Floor planning	c) Testing
b) Placement & Routing	(d) Extraction
22. In logic synthesis, is an EDIF that g	ives the description of logic cells & their
inter connections.	
(a) Netlist	c) Checklist
b) Shitlist	d) Dualist
V22 WILL 1 0 11 0 11	
23. Which among the following operation/s is/are stage?	executed in physical design or layout synthesis
Placement of logic functions in optimized cireInterconnection of components in the chip	reuit in target chip
c) Both a and b	
d) None of the above	
a) Trone of the above	
24. In synthesis flow, which stage/s is/are respons	sible for converting an un ontimized boolean
description to PLA format?	of the converting an an optimized boolean
(a) Flattening	a) Ontimization
b) Translation	c) Optimization
o, ransation	d) All of the above
25. In floorplanning, placement and routing are	
a) Front end	tools. c) Both a and b
b)Back end	(d) None of the above
	d) None of the above
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Name of the Student: T. MEENAL	Year/Sem: W/VII
AU Register Number: 91261510	66010
Value Added Course on "Di	gital System Design with Xilinx"
MCQ QUESTIO	NS (25X1 = 25 Marks)
Which of the following options comes Electronics?	under the non – saturated logic family in Digital
(a) Emitter – coupled Logic	c) Integrated – injection Logic
b) High-Threshold Logic	d) Diode – Transistor Logic
Which characteristic of IC in Digital C particular transistor?	ircuits represents a function of the switching time of a
a) Fan – out	c) Power dissipation
b) Fan – in	(d) Propagation delay
3.) Which gates in Digital Circuits are required flop? (a) Two 2 input AND gates b) Two 3 input AND gates	c) Two 2 input OR gates d) Two 3 input OR gates
4.) What must be used along with synchron	nous control inputs to trigger a change in the flip flop?
a) 0	© Clock
b) 1	d) Previous output
5. What are the basic gates in MOS logic f	family?
(a) NAND and NOR	c) NAND and OR
b) AND and OR	d) AND and NOR
6. Which of the following is only predefine	ed physical literal in VHDL?
a) Voltage	c) Current
(b) Time	d) Distance
7.) Access types are similar to i	n traditional programming languages.
(a) Pointers	c) Structures
b) Arrays	d) Files
8. Which of the following is default delay	in VHDL?
(a) Inertial delay	c) Delta delay
b) Transport delay	d) Wire delay
9. Transport delay is a kind of	Salaman and a mark and market

a) Synthesis delay b) Simulation delay c) Inertial delayr. S.THILAGAVATHI M.E., PAD. PRINCIPAL SRI BHARATHI ENGINEERING COLLEGE FOR WOMEN Kaikkurchi - 622 303, Pudukkottai Dt.

(d) Wire delay



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input A changes after 10 ns from 0 to 1 and it chatime, the value of output B will be 1, if the transp	
a) 20 ns	c) 40 ns
(B) 30 ns	d) Output will remain zero
11. The process used for implementation of sequential	al logic in VHDL is called process.
11. The process used for implementation of sequential a) Sequential process	c) Clocked process
b) Combinational process	d Unlocked process
12. A user doesn't want to use the IF statement for d	letecting clock edge. It is possible to do the
same by using any other keyword in VHDL.	
a) True	b) False
13. PLA contains	
(a) AND and OR arrays	c) NOT and AND arrays
b) NAND and OR arrays	d) NOR and OR arrays
14. A PLA is similar to a ROM in concept except tha	ne simosi) totisi (f nr zoneg dom). (s at
a) It hasn't capability to read only variables	© It doesn't provide full decoding to the
b) It hasn't capability to read or write operation	d) It hasn't capability to write only
b) It hasn't capability to read or write operation	d) It hasn't capability to write only
15. The complex programmable logic device contain	as several PLD blocks and
15. The complex programmable logic device contain a) A language compiler	s several PLD blocks and © Global interconnection matrix
15. The complex programmable logic device contain	s several PLD blocks and
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays	s several PLD blocks and © Global interconnection matrix
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are?	c Global interconnection matrix d) Field-programmable switches
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD	c) EPROM
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are?	c Global interconnection matrix d) Field-programmable switches
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD	c) EPROM d) PLD
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM	c) EPROM d) PLD
 15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are seen. 	c) EPROM d) PLD eparated by
 15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are sea a) A line b) A channel 	c) EPROM d) PLD eparated by c) A strobe d) A flip-flop
 15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are sea a) A line b) A channel 18. In a digital clock application, the basic frequency 	c) EPROM d) PLD eparated by c) A strobe d) A flip-flop
 15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are sea a) A line b) A channel 	c) EPROM d) PLD eparated by c) A strobe d) A flip-flop y must be divided down as
 15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are so a) A line b) A channel 18. In a digital clock application, the basic frequency a) 1 Hz 	c) Global interconnection matrix d) Field-programmable switches c) EPROM d) PLD eparated by c) A strobe d) A flip-flop y must be divided down as c) 100 Hz
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are sea a) A line b) A channel 18. In a digital clock application, the basic frequency a) 1 Hz b) 60 Hz	as several PLD blocks and © Global interconnection matrix d) Field-programmable switches c) EPROM © PLD eparated by c) A strobe d) A flip-flop y must be divided down as c) 100 Hz d) 1000 Hz
15. The complex programmable logic device contain a) A language compiler b) AND/OR arrays 16. Which type of device FPGA are? a) SLD b) SROM 17. In FPGA, vertical and horizontal directions are so a) A line b) A channel 18. In a digital clock application, the basic frequency a 1 Hz b) 60 Hz	as several PLD blocks and © Global interconnection matrix d) Field-programmable switches c) EPROM © PLD eparated by c) A strobe d) A flip-flop y must be divided down as c) 100 Hz d) 1000 Hz

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20. An Antifuse programming technol	ogy is predominantly associated with
a) SPLDs	c) CPLDs
(b) FPGAs	d) All of the above
	d) III of the doore
21. In VLSI design, which process design interconnections?	als with the determination of resistance & capacitance of
a) Floor planning	c) Testing
b) Placement & Routing	(d) Extraction
, , , , , , , , , , , , , , , , , , , ,	d) Distraction
22. In logic synthesis, is an inter connections.	EDIF that gives the description of logic cells & their
a) Netlist	© Checklist
b) Shitlist	d) Dualist
	a) Duariot
23. Which among the following operar stage? a) Placement of logic functions in components in Compon	
d) None of the above	
24. In synthesis flow, which stage/s is description to PLA format? a) Flattening	s/are responsible for converting an un optimized boolean © Optimization
b) Translation	d) All of the above
25 In floorplanning, placement and rou	uting are tools.
a) Front end	c) Both a and b
(b)Back end	d) None of the above
O 2	d) None of the above
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Dr. S.THILA	AGAVATHIM.E.,Ph.D.,
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DEPARTMENT OF ELECTRONICS AND COMMUNICATIONENGINEERING

ACADEMIC YEAR ODD SEMESTER (2018-2019)

MARK SHEET FOR VALUE ADDED COURSE- "DIGITAL SYSTEM DESIGN WITH XILINX"

73	2009019199003	NAME	YEAR & BRANCH		ndance (A)	VAC -MC	OVERALL MARK(100)	
S.NO	REGISTER NUMBER			No.of Sessions Attented	Marks (100)	No.of Correct Answer	Marks (100)	(50% of A + 50% of B)
1	912617106001	ABIRAMI.S	II /ECE	10	100	22	88	94
2	912617106002	ABISHEKA.S	II /ECE	10	100	23	92	96
3	912617106003	ATSHAYA.R	II /ECE	9	90	21	84	87
4	912617106004	BAVADHARANI.A	II /ECE	. 9	90	20	80	85
5	912617106005	BHUVANESHWARI.B	II /ECE	10	100	19	76	88
6	912617106006	DHIVYA.L	II /ECE	10	100	20	80	90
. 7	912617106007	GOWSALYA.D	II /ECE	10	100	21	84	92
8	912617106009	INDHUMATHI.S	II /ECE	9	90	19	76	83
9	912617106010	KANIMOZHI.D	II /ECE	10	100	18	72	86
10	912617106011	KAVYA.C	II /ECE	10	100	22	88	94
11	912617106012	KEERTHANA.G	II /ECE	10	100	20	80	90

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12	912617106013	MAHESHWARI.G	II /ECE	10	100	19	76	88
13	912617106014	MANOHARI.M	II /ECE	10	100	18	72	86
14	912617106015	MARAGATHALAKSHMI.S	II /ECE	8	80	20	80	80
15	912617106017	SAFRIN NISHA.S	II /ECE	10	100	20	80	90
16	912617106018	SUBASHINI.M	II /ECE	10	100	18	72	86
17	912617106019	SUBASHINI.T	II /ECE	8	80	19	76	78
18	912617106020	VINTHIYA.R	II /ECE	10	100	22	88	94
19	912616106001	ABINAYA.R	III /ECE	10	100	19	76	88
20	912616106002	AGALYA.A	III /ECE	8	80	18	72	76
21	912616106003	ATCHAYA.G	III /ECE	10	100	19	76	88
22	912616106004	DEEPA.N	III /ECE	10	100	22	88	94
23	912616106005	DHARANIYA.A	III /ECE	9	90	18	72	81
24	912616106006	JEEVITHA.U	III /ECE	10	100	19	76	88
25	912616106007	MAHESWARI.V	III /ECE	8	80	21	84	82
26	912616106008	PAZHANIYAMMAL.R	III /ECE	10	100	23	92	96
27	912616106009	PRIYANKA.E	III /ECE	10	100	21	84	92
28	912616106010	ROJA.A	III /ECE	10	100	23	92	96
29	912616106011	SHANMUGAPRIYA.R	III /ECE	10	100	19	76	88
30	912616106012	SHIYAMALA.E	III /ECE	10	100	19	76	88
31	912616106013	SIVA BHARATHI.P	III /ECE	10	100	18	72	86
32	912616106014	SIVARUBINI.S	III /ECE	10	100	23	82	91

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33	912616106015	THENMOZHI.A	III /ECE	8	80	18	72	76
34	912616106016	VINCY.A	III /ECE	10	100	18	72	86
35	912616106302	SANKAVI M	III /ECE	10	100	19	76	88
36	912615106001	AARTHI .M	IV/ECE	9	90	18	72	81
37	912615106002	ABIRAMI .C	IV/ECE	10	100	20	80	90
38	912615106004	AKILA .S	IV/ECE	10	100	19	76	88
39	912615106005	ARTHI .M	IV/ECE	10	100	18	72	86
40	912615106006	BAVADHARANI .M	IV/ECE	10	100	18	72	86
41	912615106007	DIVYABHARATHI .S	IV/ECE	10	100	19	76	88
42	912615106008	JAGADESWARI .K	IV/ECE	10	100	17	68	84
43	912615106009	MEENAKSHI .R	IV/ECE	8	80	19	76	78
44	912615106010	MEENAL.T	IV/ECE	10	100	21	84	92
45	912615106012	SARGUNAVALLI.C	IV/ECE	8	80	20	80	80
46	912615106013	THENMOZHI .K	IV/ECE	10	100	15	60	80
47	912615106014	VENNILA .K	IV/ECE	10	100	22	88	94
48	912615106301	MANIMEGALAI .S	IV/ECE	9	90	19	76	83
49	912615106701	SARADHA .S	IVÆCE	10	100	23	92	96
50	912615106702	KAVIYA. S	IV/ECE"	. 10	100	20	80	90

VAC Coordinator

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